



## 3.3-V / 5-V HIGH-SPEED DIGITAL ISOLATORS

### FEATURES

- **4000-V<sub>(peak)</sub> Isolation**
  - UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2)
  - IEC 61010-1 and CSA Approved
  - 50 kV/μs Transient Immunity Typical
- **Signaling Rate 0 Mbps to 150 Mbps**
  - Low-Propagation Delay
  - Low Pulse-Width Distortion
- **High-Electromagnetic Immunity**
- **Low-Input Current Requirement**
- **Failsafe Output**

- **Drop-In Replacement for Most Opto and Magnetic Isolators**

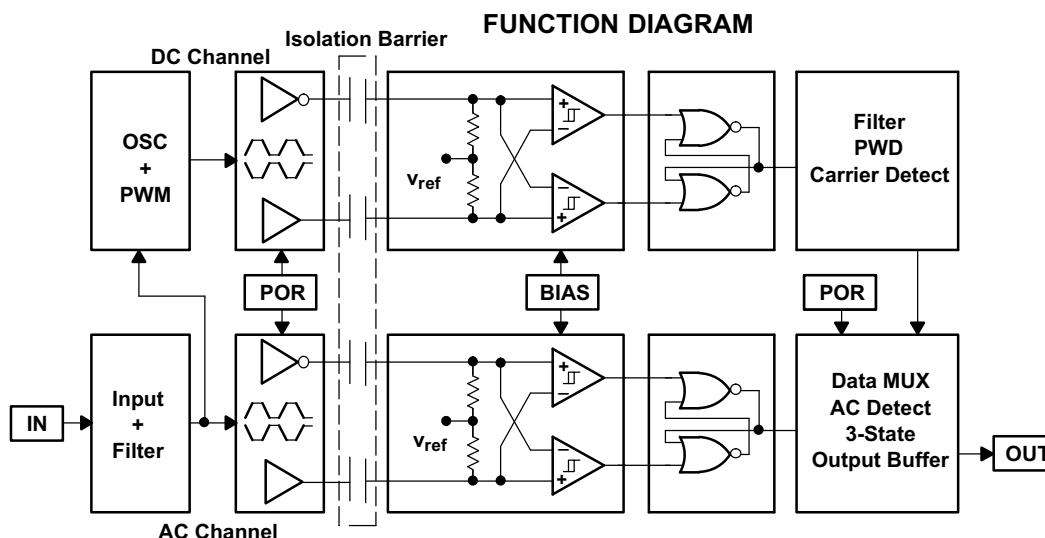
### APPLICATIONS

- **Industrial Fieldbus**
  - Modbus
  - Profibus
  - DeviceNet™ Data Buses
  - Smart Distributed Systems (SDS™)
- **Computer Peripheral Interface**
- **Servo Control Interface**
- **Data Acquisition**

### DESCRIPTION

The ISO721 and ISO721M digital isolators have a logic input and output buffer separated by a silicon oxide (SiO<sub>2</sub>) insulation barrier. This barrier provides galvanic isolation of up to 4000 V. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground, and interfering with or damaging sensitive circuitry.

A binary input signal is conditioned, translated to a balanced signal, then differentiated by the capacitive isolation barrier. Across the isolation barrier, a differential comparator receives the logic transition information, then sets or resets a flip-flop and the output circuit accordingly. A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received for more than 4 μs, the input is assumed to be unpowered or not functional, and the failsafe circuit drives the output to a logic high state.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

The symmetry of the dielectric and capacitor within the integrated circuitry provides for close capacitive matching, and allows fast transient voltage changes between the input and output grounds without corrupting the output. The small capacitance and resulting time constant provide for fast operation with signaling rates<sup>(1)</sup> from 0 Mbps (dc) to 100 Mbps for the ISO721, and 0 Mbps to 150 Mbps with the ISO721M.

These devices require two supply voltages of 3.3-V, 5-V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply and all outputs are 4-mA CMOS.

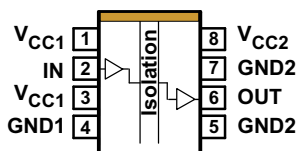
The ISO721 has TTL input thresholds and a noise-filter at the input that prevents transient pulses of up to 2 ns in duration from being passed to the output of the device.

The ISO721M has CMOS  $V_{CC}/2$  input thresholds, but does not have the noise-filter and the additional propagation delay. These features of the ISO721M also provide for reduced jitter operation.

The ISO721 and ISO721M are characterized for operation over the ambient temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

### PACKAGE PIN ASSIGNMENTS ISO721D, ISO721MD (TOP VIEW)



### ORDERING INFORMATION

PRODUCT	INPUT THRESHOLDS	NOISE FILTER	PACKAGE <sup>(1)</sup>	PACKAGE DESIGNATOR	MARKED AS	ORDERING NUMBER	GREEN
ISO721	TTL	YES	SOIC-8	D	ISO721	ISO721D (rail)	Pb Free Sb/Br Free
						ISO721DR (reel)	
ISO721M	CMOS	NO	SOIC-8	D	ISO721M	ISO721MD (rail)	
						ISO721MDR (reel)	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

### REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program <sup>(1)</sup>
File Number: 40014131	File Number: 1698195	File Number: 181974

(1) Production tested  $\geq 3000 V_{RMS}$  for 1 second in accordance with UL 1577.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)</sup>

				UNIT
$V_{CC}$	Supply voltage, $V_{CC1}$ , $V_{CC2}$			–0.5 V to 6 V
$V_I$	Voltage at IN or OUT terminal			–0.5 V to 6 V
$I_O$	Output Current			±15 mA
ESD	Electrostatic discharge	Human Body Model	JEDEC Standard 22, Test Method A114-C.01	All pins ±2 kV ±1 kV
		Charged Device Model	JEDEC Standard 22, Test Method C101	
$T_J$	Maximum junction temperature			170°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) This isolator is suitable for basic insulation applications within the safety limiting data. Maintenance of the safety data must be ensured by means of protective circuitry.

## RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT	
V <sub>CC</sub> Supply voltage, V <sub>CC1</sub> , V <sub>CC2</sub>			4.5		5.5	V	
			3		3.6		
I <sub>OH</sub>	Output current		4			mA	
I <sub>OL</sub>			-4				
t <sub>ui</sub>	Input pulse width		ISO721	10		ns	
			ISO721M	6.67			
V <sub>IH</sub>	High-level input voltage (IN)		ISO721	2	V <sub>CC</sub>	V	
V <sub>IL</sub>	Low-level input voltage (IN)			0	0.8		
V <sub>IH</sub>	High-level input voltage (IN)		IOS721M	0.7 V <sub>CC</sub>	V <sub>CC</sub>	V	
V <sub>IL</sub>	Low-level input voltage (IN)			0	0.3 V <sub>CC</sub>		
T <sub>J</sub>	Junction temperature		See the Thermal Characteristics table			150	°C
H	External magnetic field intensity per IEC 61000-4-8 and IEC 61000-4-9 certification					1000	A/m

## IEC 60747-5-2 INSULATION CHARACTERISTICS<sup>(1)</sup>

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SPECIFICATIONS	UNIT
$V_{IORM}$	Maximum working insulation voltage	560	V
$V_{PR}$	Input to output test voltage	After Input/Output Safety Test Subgroup 2/3 $V_{PR} = V_{IORM} \times 1.2$ , $t = 10$ s, Partial discharge < 5 pC	672 V
		Method a, $V_{PR} = V_{IORM} \times 1.6$ , Type and sample test with $t = 10$ s, Partial discharge < 5 pC	896 V
		Method b1, $V_{PR} = V_{IORM} \times 1.875$ , 100 % Production test with $t = 1$ s, Partial discharge < 5 pC	1050 V
$V_{IOTM}$	Transient overvoltage	$t = 60$ s	4000 V
$R_S$	Insulation resistance	$V_{IO} = 500$ V at $T_S$	$>10^9$ $\Omega$
	Pollution degree	2	

- (1) Climatic Classification 40/125/21

**ELECTRICAL CHARACTERISTICS:  $V_{CC1}$  and  $V_{CC2}$  5-V OPERATION**

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>CC1</sub>	V <sub>CC1</sub> supply current	Quiescent	V <sub>I</sub> = V <sub>CC</sub> or 0 V, No load		0.5	1	mA
		25 Mbps			2	3.5	
I <sub>CC2</sub>	V <sub>CC2</sub> supply current	Quiescent	V <sub>I</sub> = V <sub>CC</sub> or 0 V, No load		8	12	mA
		25 Mbps			10	14	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4 mA, See <a href="#">Figure 1</a>		V <sub>CC</sub> – 0.8	4.6		V
		I <sub>OL</sub> = –20 μA, See <a href="#">Figure 1</a>		V <sub>CC</sub> – 0.1	5		
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA, See <a href="#">Figure 1</a>			0.2	0.4	V
		I <sub>OL</sub> = 20 μA, See <a href="#">Figure 1</a>			0	0.1	
V <sub>I(HYS)</sub>	Input voltage hysteresis				150		mV
I <sub>IH</sub>	High-level input current	IN at 2 V				10	μA
I <sub>IL</sub>	Low-level input current	IN at 0.8 V		–10			
C <sub>I</sub>	Input capacitance to ground	V <sub>I</sub> = 0.4 sin (4E6πt) + 0.5 V			1		pF
CMTI	Common-mode transient immunity	V <sub>I</sub> = V <sub>CC</sub> or 0 V, See <a href="#">Figure 3</a>		25	50		kV/μs

**SWITCHING CHARACTERISTICS:  $V_{CC1}$  and  $V_{CC2}$  5-V OPERATION**

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t <sub>PLH</sub>	Propagation delay, low-to-high-level output	ISO721	See <a href="#">Figure 1</a>	13	17	24	ns	
t <sub>PHL</sub>	Propagation delay , high-to-low-level output			13	17	24		
t <sub>sk(p)</sub>	Pulse skew  t <sub>PHL</sub> – t <sub>PLH</sub>				0.5	2		
t <sub>PLH</sub>	Propagation delay, low-to-high-level output	ISO721M		8	10	16	ns	
t <sub>PHL</sub>	Propagation delay, high-to-low-level output			8	10	16		
t <sub>sk(p)</sub>	Pulse skew  t <sub>PHL</sub> – t <sub>PLH</sub>				0.5	1		
t <sub>sk(pp)</sub> <sup>(1)</sup>	Part-to-part skew					0	3	ns
t <sub>r</sub>	Output signal rise time			See <a href="#">Figure 1</a>		1		ns
t <sub>f</sub>	Output signal fall time					1		
t <sub>fs</sub>	Failsafe output delay time from input power loss			See <a href="#">Figure 2</a>		3		μs
t <sub>jitter(PP)</sub>	Peak-to-peak eye-pattern jitter	ISO721	100 Mbps NRZ data input See <a href="#">Figure 4</a>		2		ns	
			100 Mbps unrestricted bit run length data input See <a href="#">Figure 4</a>		3			
		ISO721M	150 Mbps NRZ data input See <a href="#">Figure 4</a>		1			
			150 Mbps unrestricted bit run length data input See <a href="#">Figure 4</a>		2			

(1)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## **ELECTRICAL CHARACTERISTICS: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V OPERATION**

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC1}$	$V_{CC1}$ supply current	Quiescent	$V_I = V_{CC}$ or 0 V, No load		0.5	1	mA
		25 Mbps			2	3.5	
$I_{CC2}$	$V_{CC2}$ supply current	Quiescent	$V_I = V_{CC}$ or 0 V, No load		4	6.5	mA
		25 Mbps			5	7.5	
$V_{OH}$	High-level output voltage	$I_{OH} = -4$ mA, See <a href="#">Figure 1</a>		$V_{CC} - 0.4$	3		V
		$I_{OH} = -20$ $\mu$ A, See <a href="#">Figure 1</a>		$V_{CC} - 0.1$	3.3		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4$ mA, See <a href="#">Figure 1</a>			0.2	0.4	V
		$I_{OL} = 20$ $\mu$ A, See <a href="#">Figure 1</a>			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
$I_{IH}$	High-level input current	IN at 2 V				10	$\mu$ A
$I_{IL}$	Low-level input current	IN at 0.8 V		-10			
$C_I$	Input capacitance to ground	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V			1		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See <a href="#">Figure 3</a>		25	40		kV/ $\mu$ s

## **SWITCHING CHARACTERISTICS: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V OPERATION**

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay, low-to-high-level output	ISO721	See <a href="#">Figure 1</a>	15	19	30	ns
t <sub>PHL</sub>	Propagation delay, high-to-low-level output			15	19	30	
t <sub>sk(p)</sub>	Pulse skew  t <sub>PHL</sub> – t <sub>PLH</sub>				0.5	3	
t <sub>PLH</sub>	Propagation delay, low-to-high-level output	ISO721M		10	12	20	ns
t <sub>PHL</sub>	Propagation delay, high-to-low-level output			10	12	20	
t <sub>sk(p)</sub>	Pulse skew  t <sub>PHL</sub> – t <sub>PLH</sub>				0.5	1	
t <sub>sk(pp)</sub> <sup>(1)</sup>	Part-to-part skew			0	5	ns	
t <sub>r</sub>	Output signal rise time	See <a href="#">Figure 1</a>		2		ns	
t <sub>f</sub>	Output signal fall time			2			
t <sub>fs</sub>	Failsafe output delay time from input power loss	See <a href="#">Figure 2</a>		3		μs	
t <sub>jit(pp)</sub>	Peak-to-peak eye-pattern jitter	ISO721	100 Mbps NRZ data input See <a href="#">Figure 4</a>	2		ns	
			100 Mbps unrestricted bit run length data input See <a href="#">Figure 4</a>	3			
		ISO721M	150 Mbps NRZ data input See <a href="#">Figure 4</a>	1			
			150 Mbps unrestricted bit run length data input See <a href="#">Figure 4</a>	2			

(1)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

**ELECTRICAL CHARACTERISTICS:  $V_{CC1}$  at 3.3-V,  $V_{CC2}$  at 5-V OPERATION**

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC1}$	$V_{CC1}$ supply current	Quiescent	$V_I = V_{CC}$ or 0 V, No load		0.3	0.5	mA
		25 Mbps			1	1.5	
$I_{CC2}$	$V_{CC2}$ supply current	Quiescent	$V_I = V_{CC}$ or 0 V, No load		8	12	mA
		25 Mbps			10	14	
$V_{OH}$	High-level output voltage	$I_{OH} = -4$ mA, See Figure 1		$V_{CC} - 0.8$	4.6		V
		$I_{OH} = -20$ $\mu$ A, See Figure 1		$V_{CC} - 0.1$	5		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4$ mA, See Figure 1			0.2	0.4	V
		$I_{OL} = 20$ $\mu$ A, See Figure 1			0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
$I_{IH}$	High-level input current	IN at 2 V				10	$\mu$ A
$I_{IL}$	Low-level input current	IN at 0.8 V		-10			
$C_I$	Input capacitance to ground	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V			1		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See Figure 3		25	40		kV/ $\mu$ s

**SWITCHING CHARACTERISTICS:  $V_{CC1}$  at 3.3-V,  $V_{CC2}$  at 5-V OPERATION**

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay, low-to-high-level output	ISO721	See <a href="#">Figure 1</a>	15	17	30	ns
t <sub>PHL</sub>	Propagation delay, high-to-low-level output			15	17	30	
t <sub>sk(p)</sub>	Pulse skew  t <sub>PHL</sub> – t <sub>PLH</sub>				0.5	2	
t <sub>PLH</sub>	Propagation delay, low-to-high-level output	ISO721M		10	12	21	ns
t <sub>PHL</sub>	Propagation delay, high-to-low-level output			10	12	21	
t <sub>sk(p)</sub>	Pulse skew  t <sub>PHL</sub> – t <sub>PLH</sub>				0.5	1	
t <sub>sk(pp)</sub> <sup>(1)</sup>	Part-to-part skew				0	5	ns
t <sub>r</sub>	Output signal rise time		See <a href="#">Figure 1</a>		1		ns
t <sub>f</sub>	Output signal fall time				1		
t <sub>fs</sub>	Failsafe output delay time from input power loss		See <a href="#">Figure 2</a>		3		μs
t <sub>jit(pp)</sub>	Peak-to-peak eye-pattern jitter	ISO721	100 Mbps NRZ data input See <a href="#">Figure 4</a>		2		ns
			100 Mbps unrestricted bit run length data input See <a href="#">Figure 4</a>		3		
		ISO721M	150 Mbps NRZ data input See <a href="#">Figure 4</a>		1		
			150 Mbps unrestricted bit run length data input See <a href="#">Figure 4</a>		2		

(1)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC1}$	$V_{CC1}$ supply current	Quiescent	$V_I = V_{CC}$ or 0 V, No load	0.3	0.5	mA
		25 Mbps		1	1.5	
$I_{CC2}$	$V_{CC2}$ supply current	Quiescent	$V_I = V_{CC}$ or 0 V, No load	4	6.5	mA
		25 Mbps		5	7.5	
$V_{OH}$	High-level output voltage	$I_{OH} = -4$ mA, See <a href="#">Figure 1</a>	$V_{CC} - 0.4$	3		V
		$I_{OH} = -20$ $\mu$ A, See <a href="#">Figure 1</a>	$V_{CC} - 0.1$	3.3		
$V_{OL}$	Low-level output voltage	$I_{OL} = 4$ mA, See <a href="#">Figure 1</a>		0.2	0.4	V
		$I_{OL} = 20$ $\mu$ A, See <a href="#">Figure 1</a>		0	0.1	
$V_{I(HYS)}$	Input voltage hysteresis			150		mV
$I_{IH}$	High-level input current	IN at 2 V			10	$\mu$ A
$I_{IL}$	Low-level input current	IN at 0.8 V	-10			
$C_I$	Input capacitance to ground	$V_I = 0.4 \sin(4E6\pi t) + 0.5$ V		1		pF
CMTI	Common-mode transient immunity	$V_I = V_{CC}$ or 0 V, See <a href="#">Figure 3</a>	25	40		kV/ $\mu$ s

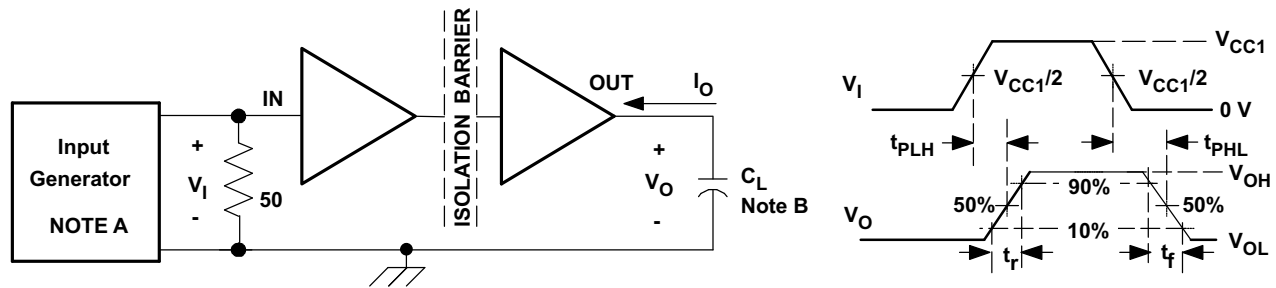
## SWITCHING CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay, low-to-high-level output	See <a href="#">Figure 1</a>	17	20	34	ns
$t_{PHL}$	Propagation delay, high-to-low-level output		17	20	34	
$t_{sk(p)}$	Pulse skew $ t_{PHL} - t_{PLH} $			0.5	3	
$t_{PLH}$	Propagation delay, low-to-high-level output	ISO721M	10	12	25	ns
$t_{PHL}$	Propagation delay, high-to-low-level output		10	12	25	
$t_{sk(p)}$	Pulse skew $ t_{PHL} - t_{PLH} $			0.5	1	
$t_{sk(pp)}^{(1)}$	Part-to-part skew			0	5.5	ns
$t_r$	Output signal rise time	See <a href="#">Figure 1</a>		2		ns
$t_f$	Output signal fall time			2		
$t_{fs}$	Failsafe output delay time from input power loss	See <a href="#">Figure 2</a>		3		$\mu$ s
$t_{jit(pp)}$	Peak-to-peak eye-pattern jitter	ISO721	100 Mbps NRZ data input See <a href="#">Figure 4</a>		2	ns
			100 Mbps unrestricted bit run length data input See <a href="#">Figure 4</a>		3	
		ISO721M	150 Mbps NRZ data input See <a href="#">Figure 4</a>		1	
			150 Mbps unrestricted bit run length data input See <a href="#">Figure 4</a>		2	

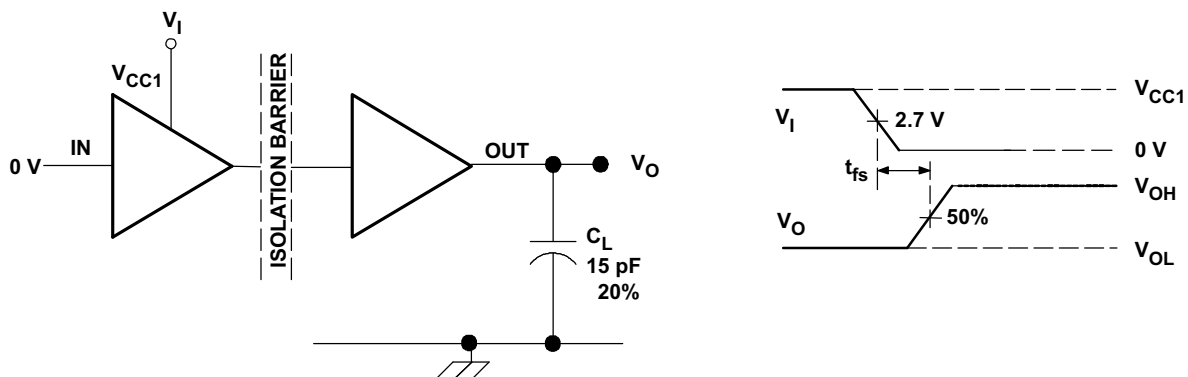
(1)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## PARAMETER MEASUREMENT INFORMATION



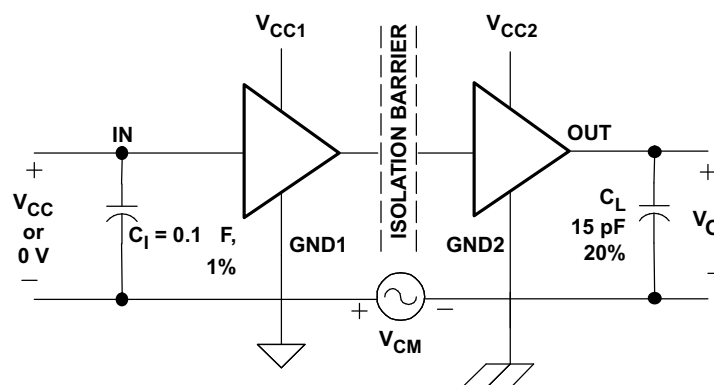
- A. The input pulse is supplied by a generator having the following characteristics:
- $PRR \leq 50\text{ kHz}$ , 50% duty cycle
  - $t_r \leq 3\text{ ns}$
  - $t_f \leq 3\text{ ns}$
  - $Z_O = 50\ \Omega$ .
- B.  $C_L = 15\text{ pF}$  and includes instrumentation and fixture capacitance within  $\pm 20\%$ .

**Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms**



NOTE:  $V_I$  transition time is 100 ns

**Figure 2. Failsafe Delay Time Test Circuit and Voltage Waveforms**

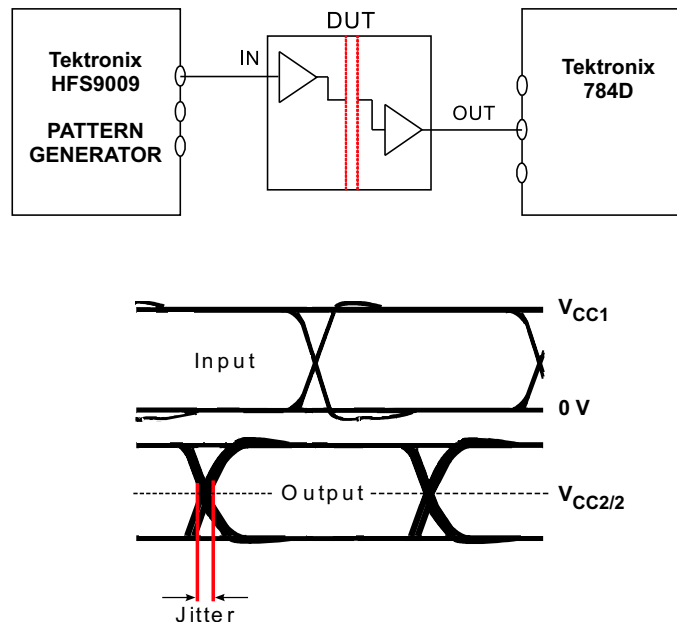


NOTE: Pass/Fail criteria is no change in  $V_O$ .

**Figure 3. Common-Mode Transient Immunity Test Circuit and Voltage Waveform**



## PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: Bit pattern run length is  $2^{16} - 1$ . Transition Time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

**Figure 4. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform**

**DEVICE INFORMATION**

**PACKAGE CHARACTERISTICS**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(101) Minimum air gap (Clearance) <sup>(1)</sup>	Shortest terminal to terminal distance through air	4.8			mm
L(102) Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	4.3			mm
C <sub>TI</sub> Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 Part 1	≥ 175			V
Minimum internal gap (internal clearance)	Distance through insulation	0.008			mm
R <sub>IO</sub> Isolation resistance	Input to output, V <sub>IO</sub> = 500 V, all pins on each side of the barrier tied together creating a two-terminal device		>10 <sup>12</sup>		Ω
C <sub>IO</sub> Barrier capacitance Input-to-output	V <sub>I</sub> = 0.4 sin (4E6πt)		1		pF
C <sub>I</sub> Input capacitance to ground	V <sub>I</sub> = 0.4 sin (4E6πt)		1		pF

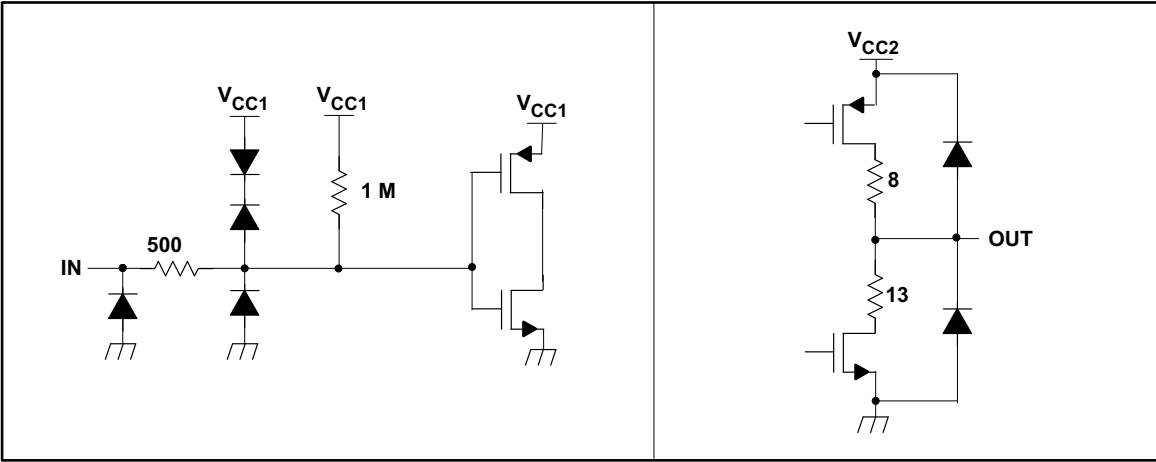
- (1) Creepage and clearance requirements are applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance. Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

**IEC 60664-1 RATINGS TABLE**

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	IIIa
Installation classification	Rated mains voltage ≤150 VRMS	I-IV
	Rated mains voltage ≤300 VRMS	I-III

**DEVICE I/O SCHEMATIC**

**Equivalent Input and Output Schematic Diagrams**



## IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolator barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply, and without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

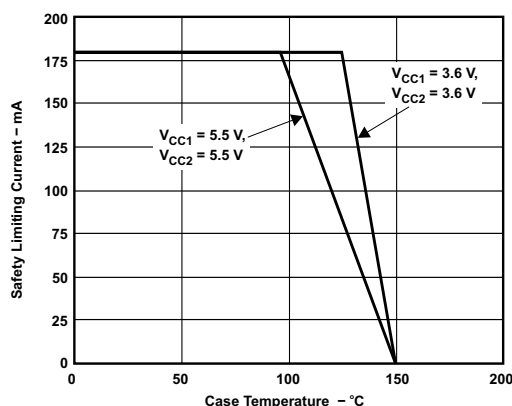
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	$\theta_{JA} = 263^{\circ}\text{C/W}$ , $V_I = 5.5\text{ V}$ , $T_J = 170^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$			100	mA
		$\theta_{JA} = 263^{\circ}\text{C/W}$ , $V_I = 3.6\text{ V}$ , $T_J = 170^{\circ}\text{C}$ , $T_A = 25^{\circ}\text{C}$			153	
T <sub>S</sub>	Maximum case temperature				150	$^{\circ}\text{C}$

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The junction-to-air thermal resistance in the Thermal Characteristics table is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

## THERMAL CHARACTERISTICS (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\theta_{JA}$	Junction-to-Air	Low-K Thermal Resistance <sup>(1)</sup>		263		$^{\circ}\text{C/W}$
		High-K Thermal Resistance <sup>(1)</sup>		125		$^{\circ}\text{C/W}$
$\theta_{JB}$	Junction-to-Board Thermal Resistance			44		$^{\circ}\text{C/W}$
$\theta_{JC}$	Junction-to-Case Thermal Resistance			75		$^{\circ}\text{C/W}$
P <sub>D</sub>	Device Power Dissipation	ISO721 $V_{CC1} = V_{CC2} = 5.5\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $C_L = 15\text{ pF}$ , Input a 100 Mbps 50% duty cycle square wave			159	mW
		ISO721M $V_{CC1} = V_{CC2} = 5.5\text{ V}$ , $T_J = 150^{\circ}\text{C}$ , $C_L = 15\text{ pF}$ , Input a 150 Mbps 50% duty cycle square wave			195	

(1) Tested in accordance with the Low-K or High-K thermal metric definition of EIA/JESD51-3 for leaded surface mount packages.



**Figure 5.  $\theta_{JC}$  THERMAL DERATING CURVE per IEC 60747-5-2**

## FUNCTION TABLE

ISO721 and ISO721M<sup>(1)</sup>

$V_{CC1}$	$V_{CC2}$	INPUT (IN)	OUTPUT (OUT)
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H
PU	PD	X	X

(1) PU = Powered Up ( $V_{CC} \geq 3$  V); PD = Powered Down ( $V_{CC} \leq 2.5$  V); X = Irrelevant; H = High Level; L = Low Level

## TYPICAL CHARACTERISTICS

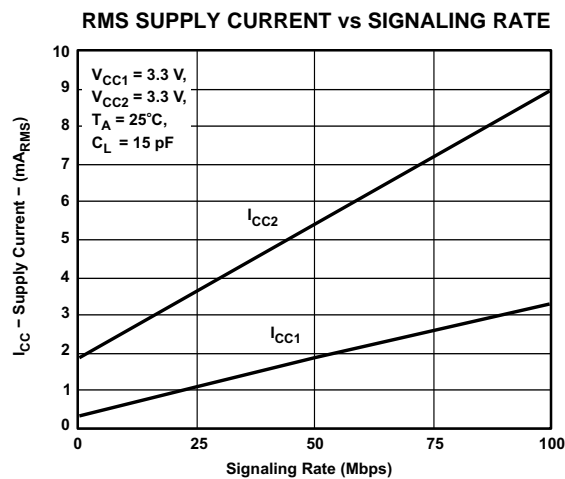


Figure 6.

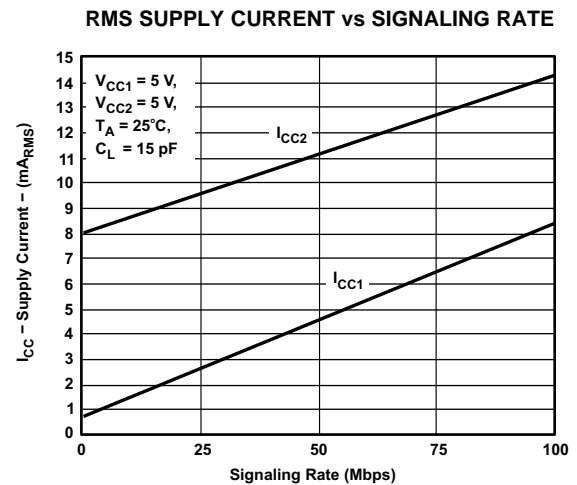


Figure 7.

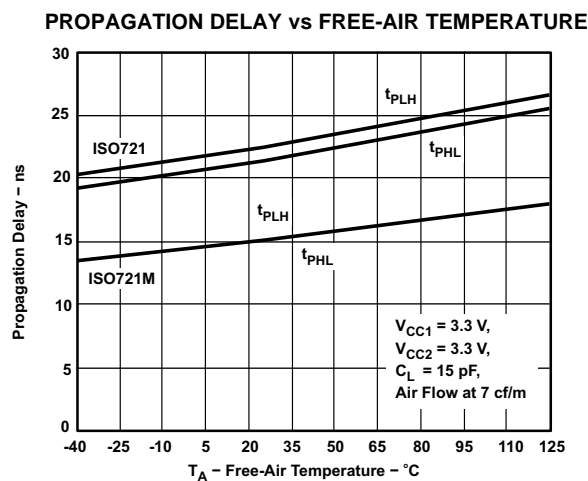


Figure 8.

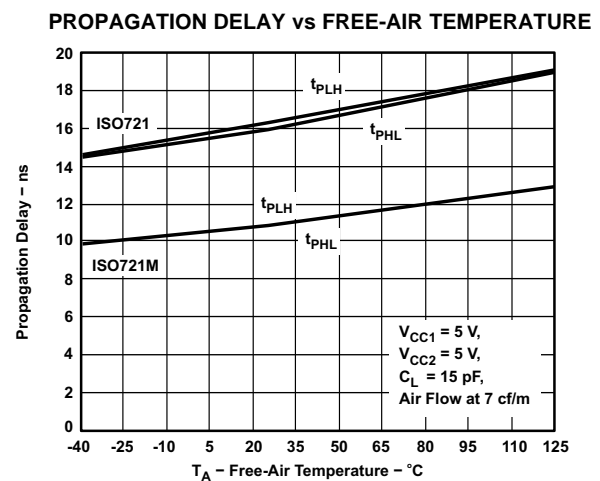
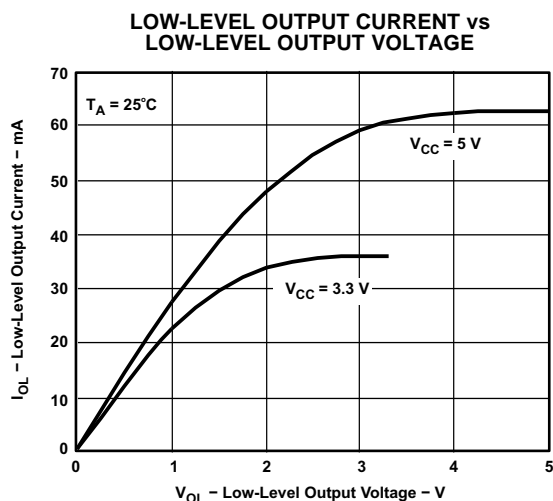
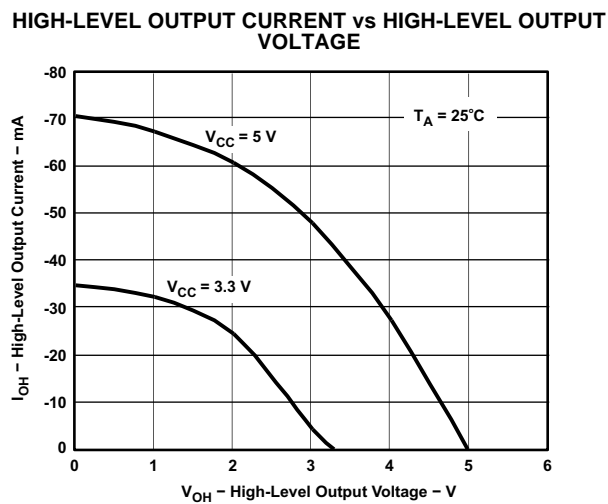
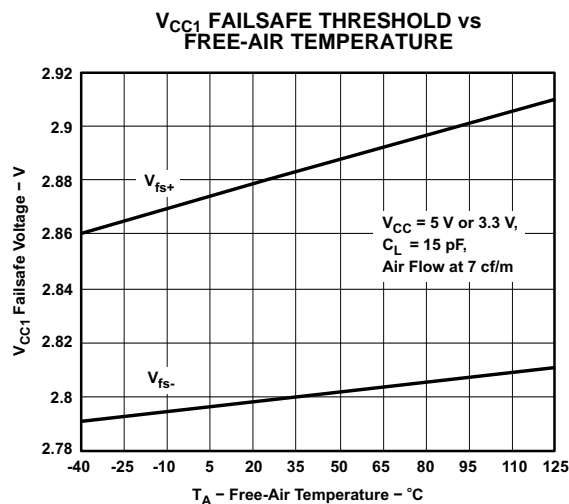
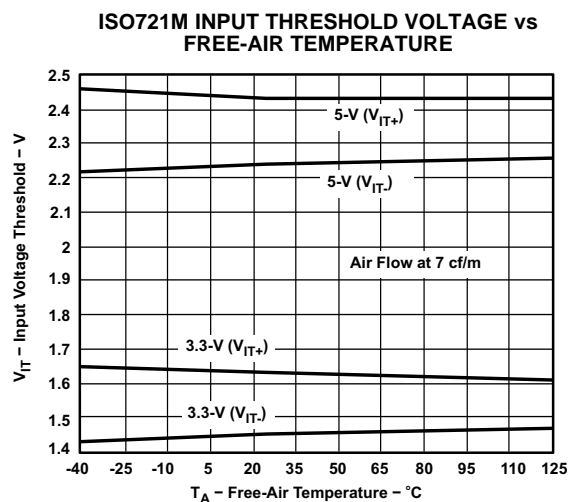
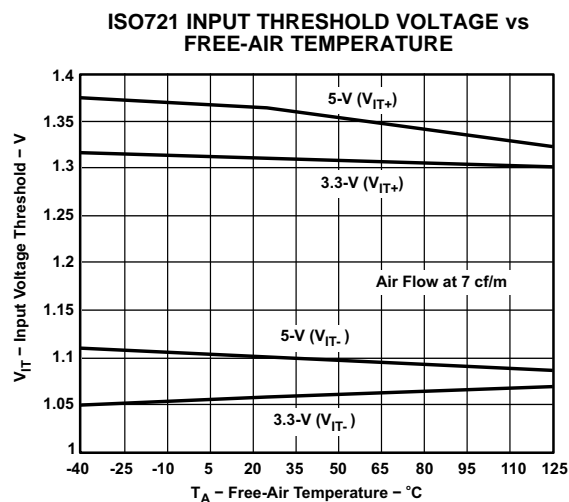


Figure 9.

## TYPICAL CHARACTERISTICS (continued)



APPLICATION INFORMATION

MANUFACTURER CROSS-REFERENCE DATA

The ISO721 and ISO721M isolators have the same functional pin-out as most other vendors, and they are often pin-for-pin drop-in replacements. The notable differences in the products are propagation delay, signaling rate, power consumption, and transient protection rating. Table 1 is used as a guide for replacing other isolators with the ISO72xx family of single channel isolators.

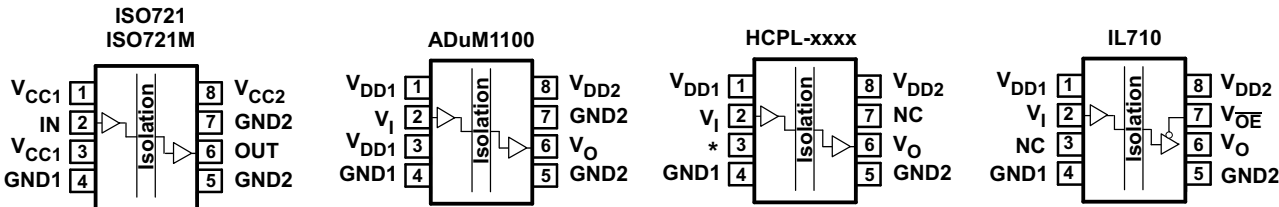


Figure 15. Pin Cross Reference

Table 1. CROSS REFERENCE

ISOLATOR	PIN 1	PIN 2	PIN 3	PIN 4	PIN 5	PIN 6	PIN 7	PIN 8
ISO721 <sup>(1)(2)</sup>	V <sub>CC1</sub>	IN	V <sub>CC1</sub>	GND1	GND2	OUT	GND2	V <sub>CC2</sub>
ADuM1100 <sup>(1)(2)</sup>	V <sub>DD1</sub>	V <sub>I</sub>	V <sub>DD1</sub>	GND1	GND2	V <sub>O</sub>	GND2	V <sub>DD2</sub>
HCPL-xxxx	V <sub>DD1</sub>	V <sub>I</sub>	*Leave Open <sup>(3)</sup>	GND1	GND2	V <sub>O</sub>	NC	V <sub>DD2</sub>
IL710	V <sub>DD1</sub>	V <sub>I</sub>	NC <sup>(4)</sup>	GND1	GND2	V <sub>O</sub>	V <sub>OE</sub>	V <sub>DD2</sub>

- (1) The ISO721 and ISO721M pin 1 and pin 3 are internally connected together. Either or both may be used as V<sub>CC1</sub>.  
(2) The ISO721 and ISO721M pin 5 and pin 7 are internally connected together. Either or both may be used as GND2.  
(3) Pin 3 of the HCPL devices must be left open. This is not a problem when substituting an ISO721 or ISO721M device since the extra V<sub>CC1</sub> on pin 3 may be left an open circuit as well.  
(4) Pin 3 of the IL710 must not be tied to ground on the circuit board since this shorts the ISO721 and ISO721M V<sub>CC1</sub> to ground. The IL710 pin 3 may only be tied to V<sub>CC</sub> or left open to drop in an ISO721 or ISO721M.

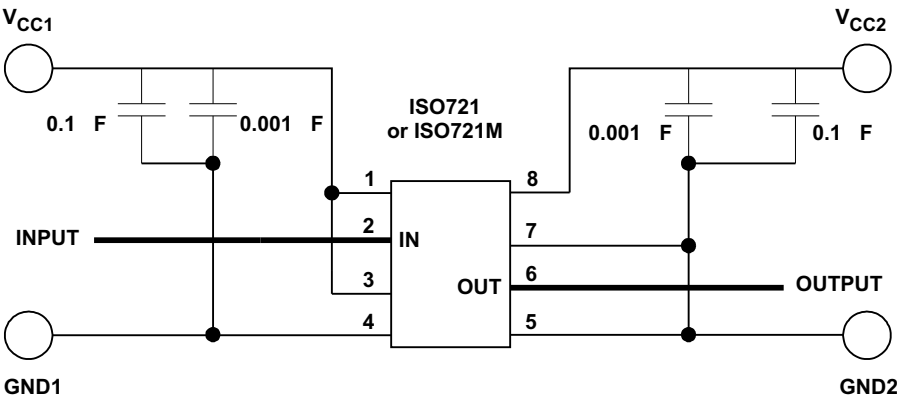
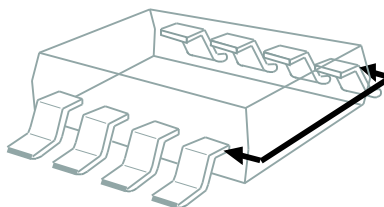


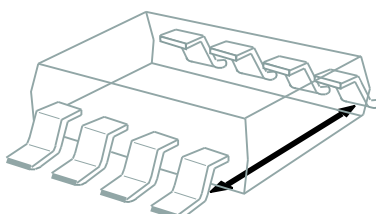
Figure 16. Basic Application Circuit

## ISOLATION GLOSSARY

**Creepage Distance**— The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



**Clearance**— The shortest distance between two conductive input to output leads measured through air (line of sight).



**Input-to Output Barrier Capacitance** -- The total capacitance between all input terminals connected together, and all output terminals connected together.

**Input-to Output Barrier Resistance** -- The total resistance between all input terminals connected together, and all output terminals connected together.

**Primary Circuit** -- An internal circuit directly connected to an external supply mains or other equivalent source which supplies the primary circuit electric power.

**Secondary Circuit** -- A circuit with no direct connection to primary power, and derives its power from a separate isolated source.

**Comparative Tracking Index (CTI)** -- CTI is an index used for electrical insulating materials which is defined as the numerical value of the voltage which causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface -- the higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as *tracking*.

**ISOLATION GLOSSARY (continued)****Insulation:**

*Operational insulation* -- Insulation needed for the correct operation of the equipment.

*Basic insulation* -- Insulation to provide basic protection against electric shock.

*Supplementary insulation* -- Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

*Double insulation* -- Insulation comprising both basic and supplementary insulation.

*Reinforced insulation* -- A single insulation system which provides a degree of protection against electric shock equivalent to double insulation.

**Pollution Degree:**

*Pollution Degree 1* -- No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence.

*Pollution Degree 2* -- Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation must be expected.

*Pollution Degree 3* -- Conductive pollution occurs or dry nonconductive pollution occurs which becomes conductive due to condensation which is to be expected.

*Pollution Degree 4* -- Continuous conductivity occurs due to conductive dust, rain, or other wet conditions.

**Installation Category:**

*Overvoltage Category* -- This section is directed at insulation co-ordination by identifying the transient overvoltages which may occur, and by assigning 4 different levels as indicated in IEC 60664.

I: Signal Level -- Special equipment or parts of equipment.

II: Local Level -- Portable equipment etc.

III: Distribution Level -- Fixed installation

IV: Primary Supply Level -- Overhead lines, cable systems

Each category should be subject to smaller transients than the category above.



## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
ISO721D	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI
ISO721DR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI
ISO721MD	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI
ISO721MDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

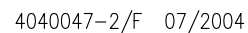
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-012 variation AA.

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