ANALOG DEVICES

AN-707
APPLICATION NOTE

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*i*Coupler® ESD and Latch-Up Considerations

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Analog Devices' family of *i*Coupler digital isolators provides an alternative isolation solution to the traditional approach involving optocouplers. In general, *i*Coupler products offer performance, power consumption, size, reliability, and cost advantages relative to optocouplers. With their digital interfaces, *i*Coupler products are easier to use than optocouplers, negating the need to drive current into an LED, bias an output transistor, or deal with a varying or poorly constrained current transfer ratio.

However, because *i*Coupler devices are fabricated using a high speed CMOS semiconductor process, care must be taken to avoid latch-up or ESD damage. This application note provides guidance and recommendations on these topics.

INTRODUCTION

Under typical conditions, *i*Coupler products are no more susceptible to ESD damage or latch-up than other CMOS components. However, since *i*Coupler products involve connections to circuitry with differing common-mode voltages, additional care must be taken to avoid ESD damage or latch-up. Table I shows a summary of the ESD testing that the ADuM130x/ADuM140x family was subjected to during product qualification. Table II contains a summary of the latch-up testing that the ADuM130x/ADuM140x family was subjected to during product qualification. Additional details can be found in the ADuM130x or ADuM140x Reliability Report.

Table I. ADuM130x/ADuM140x ESD Qualification Results

ESD Model	Highest Pass Voltage (V)	First Fail Voltage (V)
Field-Induced Charged Device Model	1500	2000
Human Body Model	3500	4000
Machine Model	200	400

Table II. ADuM130x/ADuM140x Latch-up Qualification Results

Condition	Pulse Magnitude
Current Pulses (50 μs rise time, 5 ms duration)	+102 mA, –100 mA
Voltage Pulses (50 μs rise time, 5 ms duration)	9.75 V

When an *i*Coupler is incorporated into a system design, it is possible for the above conditions to be exceeded inadvertently due to interactions between the system and the *i*Coupler device. Figure 1 shows a generalized diagram of an *i*Coupler device in a system along with the various stray capacitances C1, C2, C3, and C4 that are present. Also shown are bypass capacitors (C_{BP1} and C_{BP2}) recommended for use with *i*Coupler products. If stray capacitances are too large or accounted for improperly, they can cause ESD damage or latch-up on an *i*Coupler device. This is discussed in detail in the ESD and Latch-Up sections that follow.

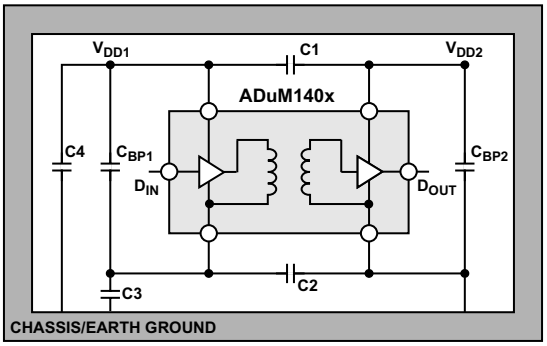

Figure 1. An iCoupler Device in a System with Stray and Bypass Capacitances

LATCH-UP

Unlike most optocoupler devices, *i*Coupler products have CMOS interfaces. As a result, precautions should be taken (as with any CMOS component) to avoid a latch-up condition. The ADuM130x/ADuM140x Data Sheets cite a voltage of 7.0 V as an absolute maximum rating on the supply pins to avoid latch-up. Such a voltage could be generated either by noise on the supply lines or by excessive stray capacitances present during electrical testing. In both cases, good bypassing (C_{BP1} and C_{BP2}) helps mitigate these effects. A value of between 0.01 μF and 0.1 μF is recommended, with these capacitors placed as close as possible to the *i*Coupler component.

Figure 2 shows the effect of stray capacitances when the system is subjected to electrical testing, such as the surge test of IEC 61000-4-5. This test calls for an ac test voltage of up to 4 kV. The impact of excessive stray capacitance between the ADuM140x and the system ground can be to induce an incremental voltage on the ADuM140x's supply pin that could cause latch-up.

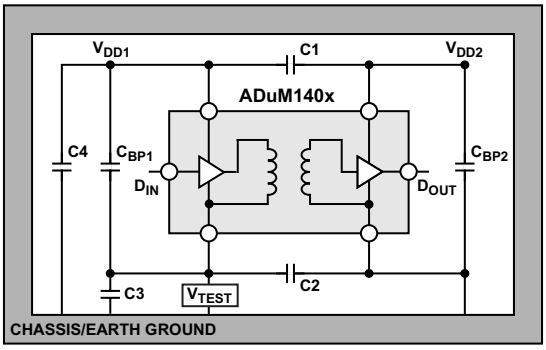

Figure 2. iCoupler Device with Stray Capacitances in the Presence of a Surge Test Voltage

The stray capacitances shown in Figure 2 between the system ground and the ADuM140x's V_{DD1} pin provide a path for a fraction of the test voltage to get induced on the V_{DD1} pin. The simplified model is shown in Figure 3.

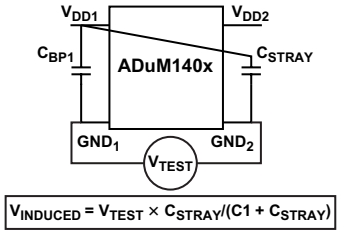

Figure 3. Simplified Model Showing Effect of Stray Capacitances

Using the terms of Figure 2, the total stray capacitance is given by:

$$C_{STRAY} = C4 + C_{BP2} \,||\, C1$$

If C_{STRAY} is small compared to C_{BP1}, the induced voltage is negligible. However, if C_{STRAY} is large (due to system shielding perhaps or a poor board layout) or C_{BP1} is small (due to inadequate bypassing), several volts can be induced at the V_{DD1} pin. This voltage is incremental to the dc supply voltage and can cause the ADuM140x to latch up.

The precautions to take against this possibility are

- Minimize the stray capacitances between an *i*Coupler device and the system ground as well as stray capacitance across the *i*Coupler device's isolation barrier
- Provide adequate bypassing as close as possible to the *i*Coupler device's pins
- Ensure supply voltages are as free as possible of noise and spikes

ESD

Although *i*Coupler devices contain ESD protection circuitry, appropriate ESD precautions should nonetheless be employed to avoid ESD-related damage. Furthermore, appropriate decoupling between *i*Coupler and system grounds should be employed to prevent system-level ESD transients from affecting the *i*Coupler device. Such decoupling typically involves adding inductance in the path between the system and *i*Coupler grounds. A more extreme solution involves the use of transient voltage suppressors known as TranZorbs. The key is to ensure the high, fast transients that the system chassis may experience are not imposed directly on the *i*Coupler device or across the isolation barrier.

BYPASS CAPACITORS

The decoupling capacitors of Figure 1 (C_{BP1} and C_{BP2}) have already been discussed in the context of avoiding latch-up. Their use is also strongly recommended to minimize supply voltage perturbations due to the *i*Coupler device's internal operation. An *i*Coupler device transmits short pulses internally to its transformers on every input logic transition. Each time one of these pulses is generated, the external supply experiences a sharp change in load and can experience a perturbation as a result. The use of adequate bypassing helps mitigate against this effect.

Such bypassing should be placed as close as possible to the *i*Coupler component. A value of between 0.01 μF and 0.1 μF is recommended, as is the use of low ESL (equivalent series inductance) capacitors such as ceramic capacitors. It should be noted that many *i*Coupler products have two ground pins on one or both sides. When present, these are internally connected to each other via the lead frame. It is strongly recommended that both pins be externally connected to each other to minimize any impact of lead/bond wire inductances.

CONCLUSIONS

Analog Devices' *i*Coupler components have been qualified to ESD and latch-up criteria commonly found with CMOS devices. However, since *i*Coupler products are isolation devices bridging a galvanic barrier between two common-mode voltages, it is possible for system-level effects to cause ESD damage or latch-up. This could be caused by excessive stray capacitances across the isolation barrier, inadequate decoupling between *i*Coupler and system grounds, inadequate bypassing, or a combination of these factors.

The user should observe the following precautions when using *i*Coupler products:

- Minimize the stray capacitances between an *i*Coupler device and the system ground as well as stray capacitance across the *i*Coupler device's isolation barrier
- Provide adequate bypassing as close as possible to the *i*Coupler device's pins
- Ensure supply voltages are as free as possible of noise, spikes, and so on
- Provide adequate decoupling between *i*Coupler device and system grounds

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