Advanced EMC

Part 2

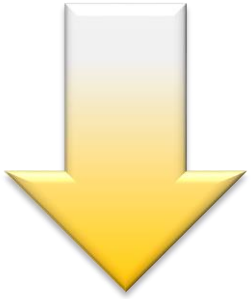
Now… this is what will happen to your designs in real life!

Agenda

- Global Approach
- Schematic Design for EMC - RF Immunity Countermeasures
- Schematic Design for EMC - RF Emissions Countermeasures
- Schematic Design for EMC – ESD Countermeasures
- Slew Rate Control
- Coupling Mechanisms
- PCB Layout – EMC overview

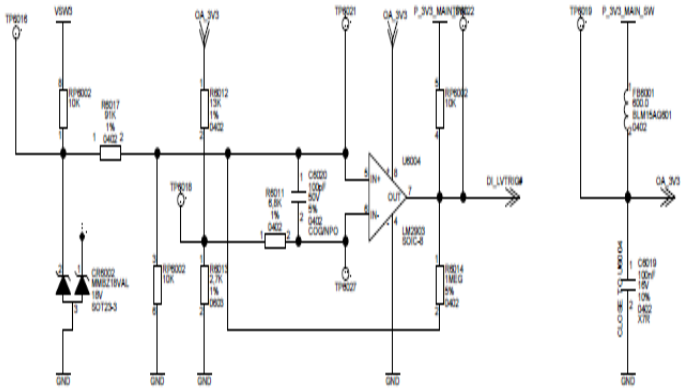
Schematic Design for EMC
Global Approach

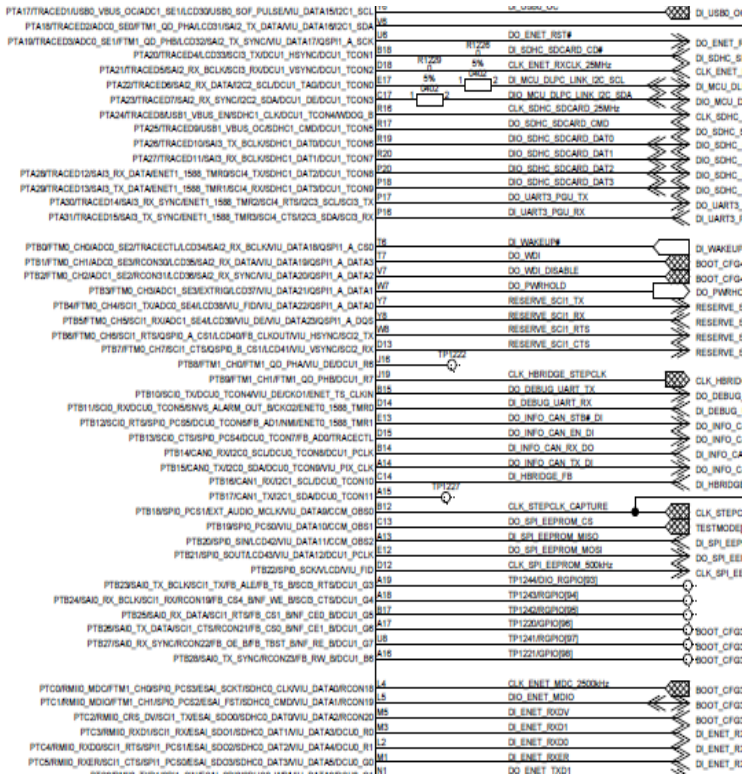
- Understand the types of EMC issues that can occur based on product content



- Then, provide EMC components in the schematic to address the issues
  - In early ED phases, provide additional components for testing purposes
  - Use ED pre-compliance phase to optimize component values
  - In late ED phases or early DV, verify & remove unneeded components

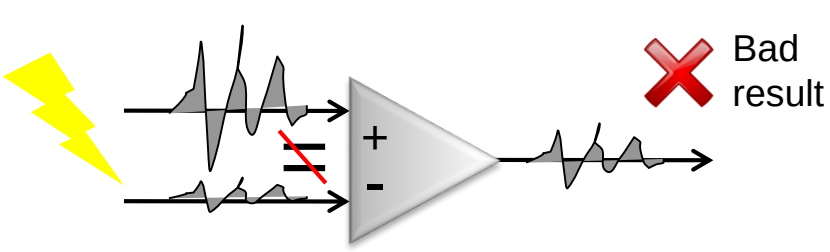
Shematic design – EMC overview Immunity



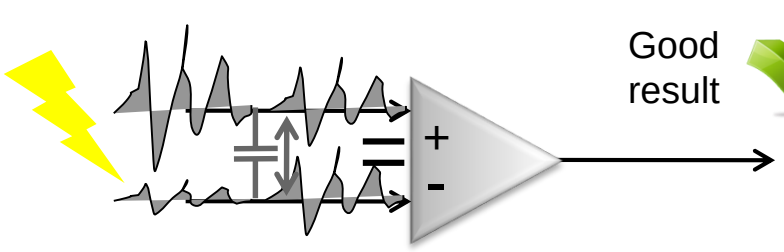


RF Immunity Countermeasures – Operational Amplifier

- Operational amplifiers have high impedance inputs
- High impedance inputs are sensitive to capacitive coupling and electric fields
- Implementation of op-amp inputs in PCB layout lines is always asymmetrical
  - Physical asymmetry is a common-mode → differential mode converter
  - If noise source is within op-amp frequency bandwidth, it will be amplified



Bad result



Good result

- Provide a 47pf – 100pf value capacitor between the input terminals
- Common mode rejection of op-amp is very good

RF Immunity Countermeasures – SMPS Controller

- SMPS controllers are sensitive to interference
- Why? → They use an error amplifier to control the output.

DEVICE INFORMATION

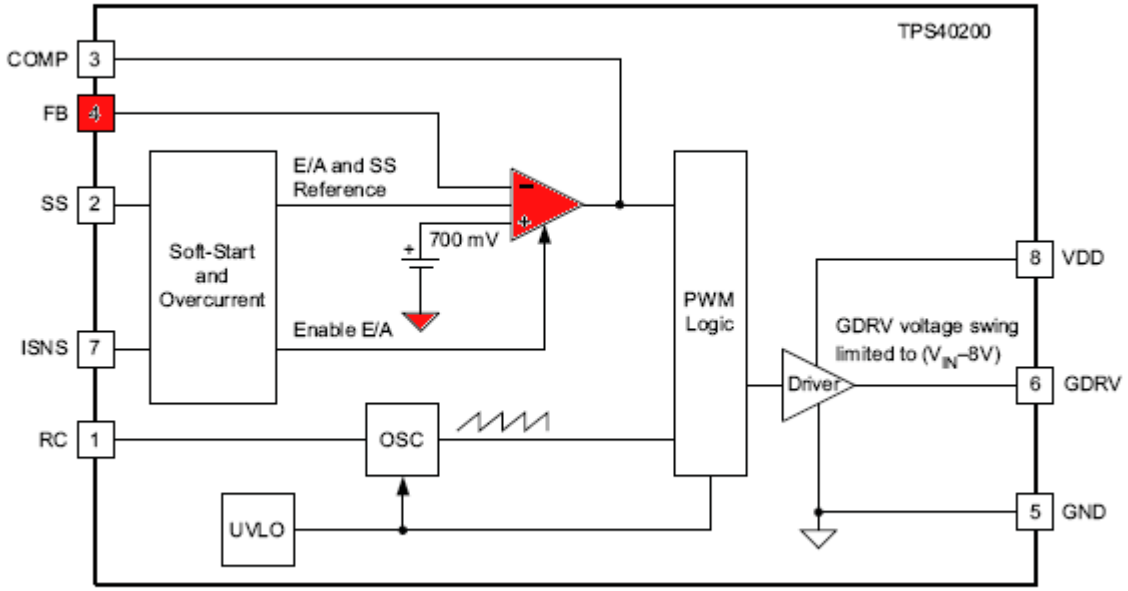
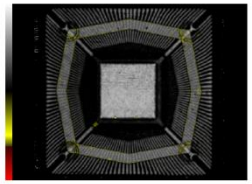


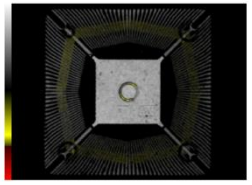
Figure 3. Functional Block Diagram

- Ford cluster program used TPS40200
- Sensitive error amplifier caused major issues due to EMC interference

- Under-voltage caused loss of pointer illumination and TFT going dark
- Over-voltage caused malfunctions and ***burned internal micro pins***

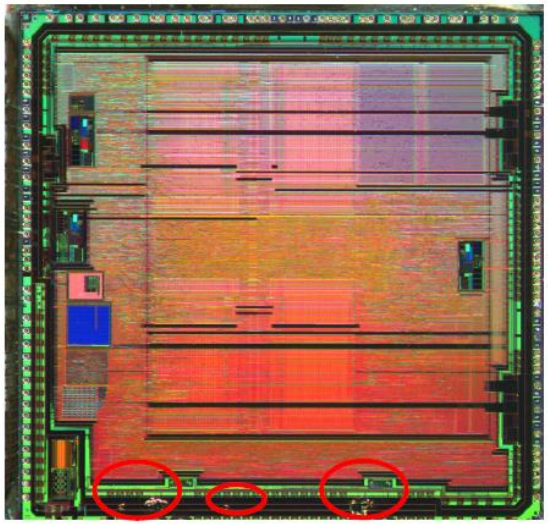
Package

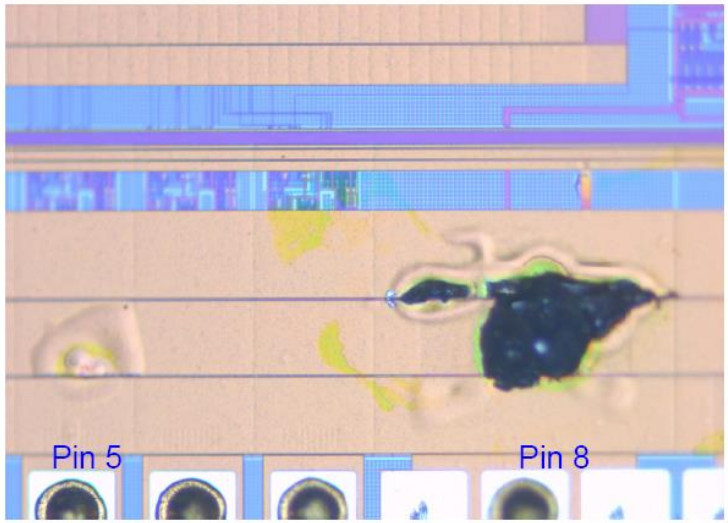

Die


Lead frame backside

D4.6 Optical inspection after decapsulation

After decapsulation, the device was examined with an optical microscope. Abnormalities were found as the following images reveal:


Whole die: 3 abnormalities



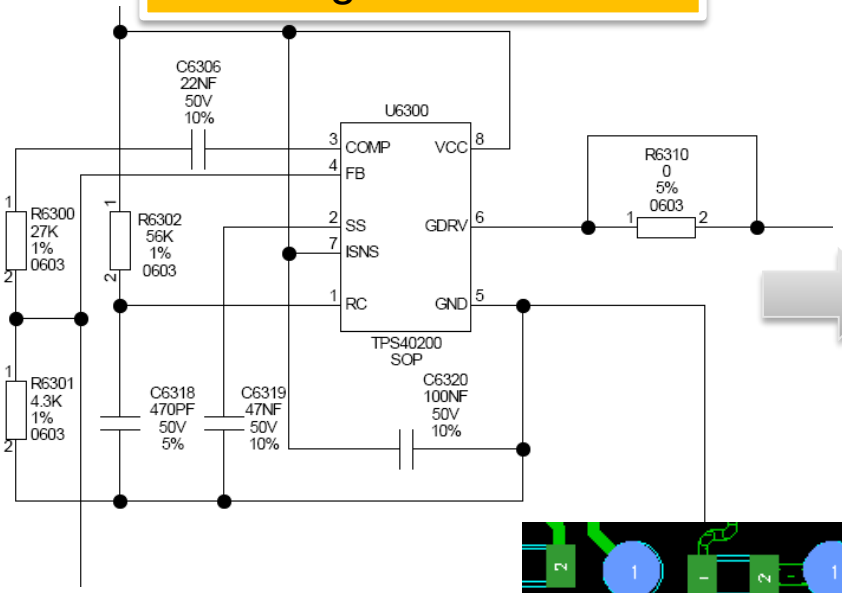
Pin 5-8: melted metal lines and carbonisation

Schematic Design for EMC

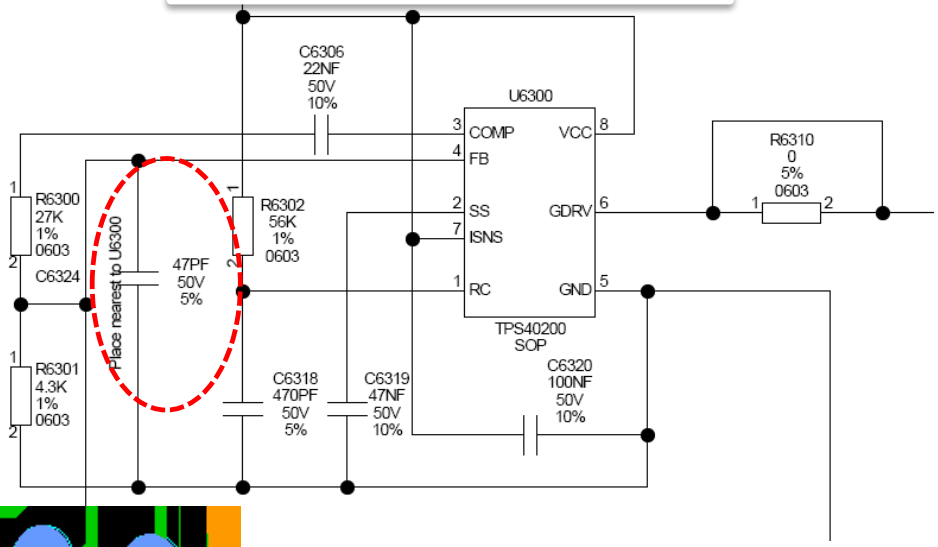
RF Immunity Countermeasures – SMPS Controller

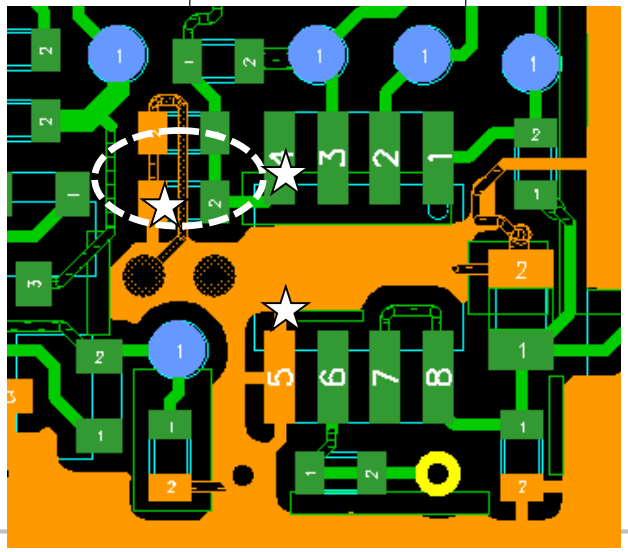
- Buck regulator circuit improvement → add 47pf cap

Original Circuit



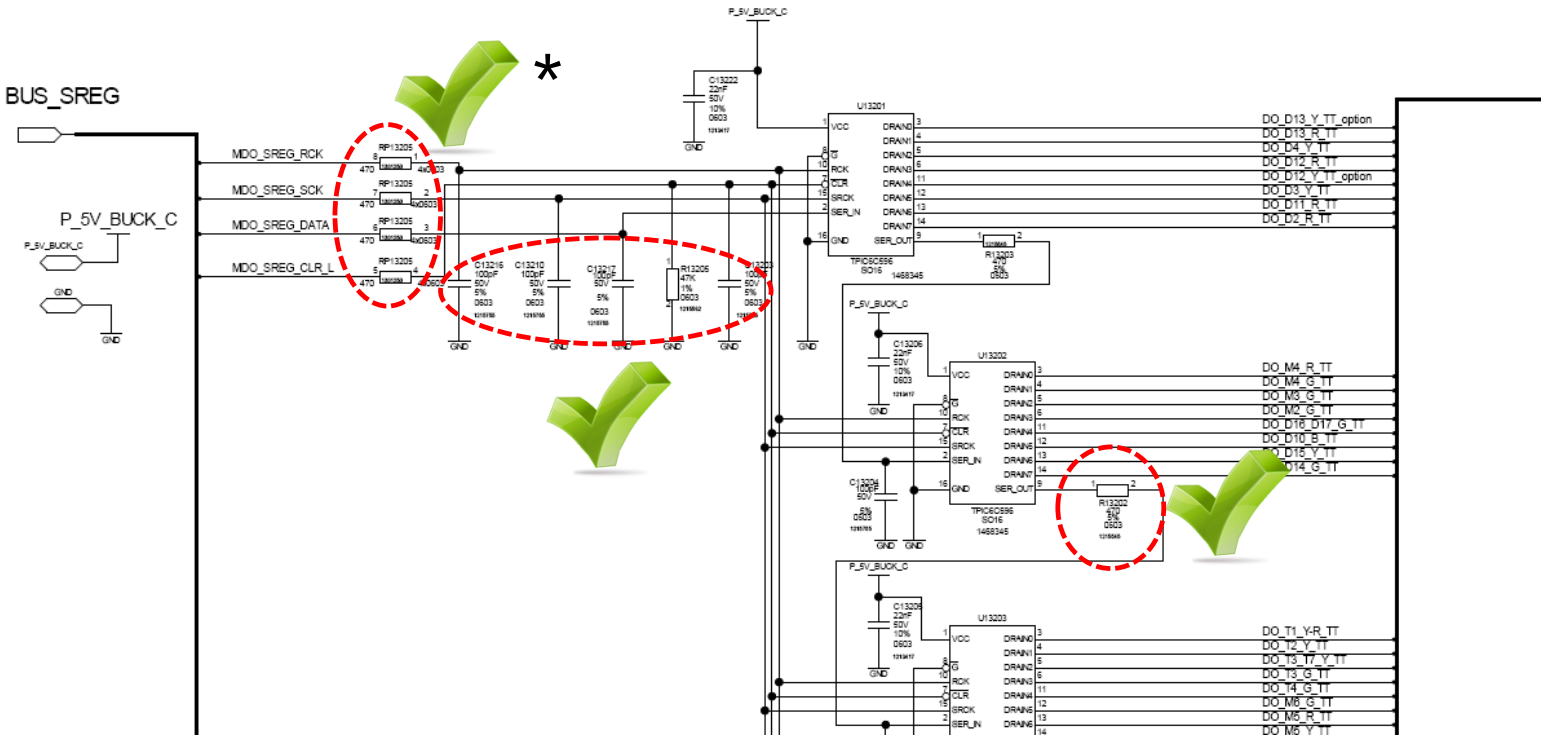
Improved Circuit





Schematic Design for EMC
RF Immunity Countermeasures – LED Shift Registers

- Shift registers are used to control many LEDs / Telltales with few uC ports
- Usually traces routed between uC and shift registers are long
- 2 layer and silver strap boards typically do not allow solid ground guard traces



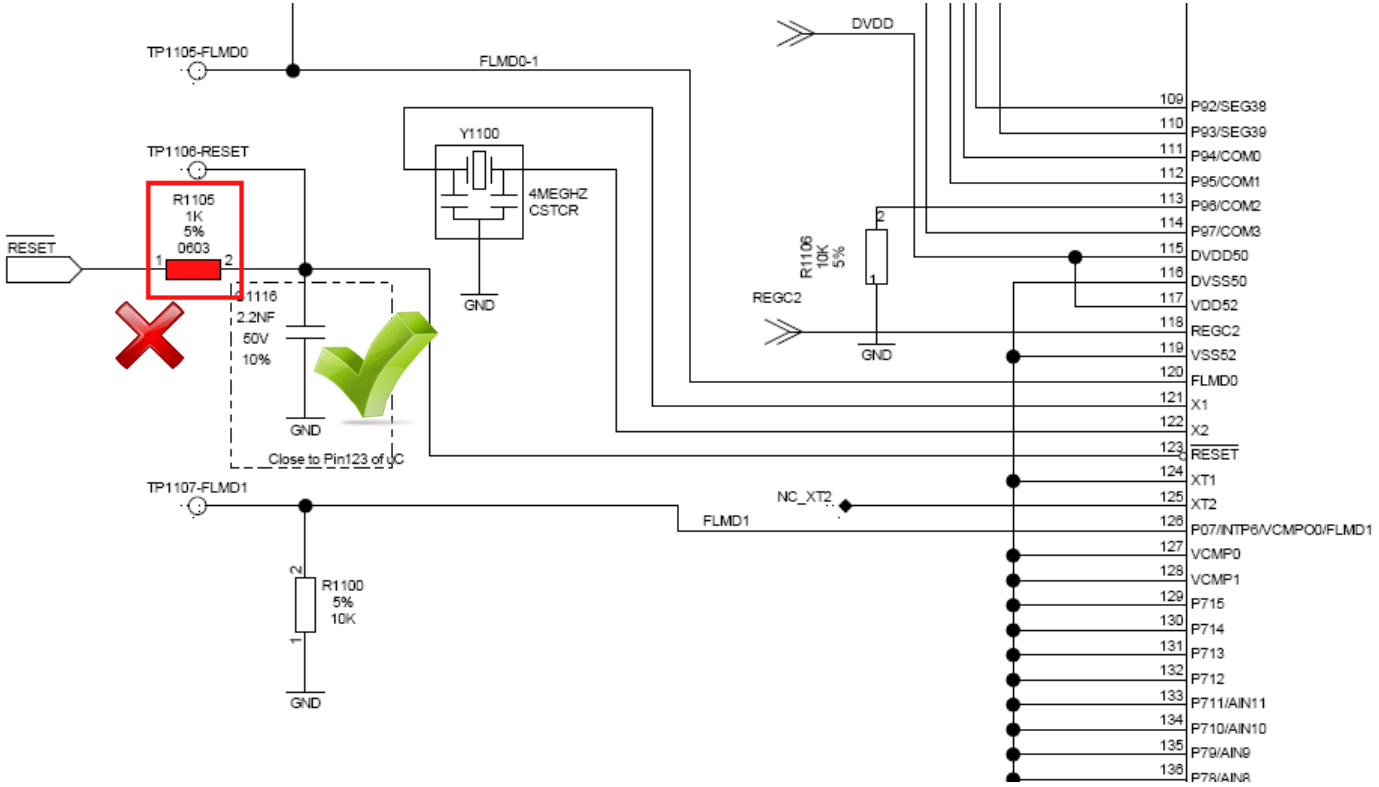
* Ferrites may be needed for RF immunity issues

RF Immunity Countermeasures – Reset Lines

- Generally a reset capacitor is placed from the reset line to ground
- Default values range from 1nf – 4.7nf

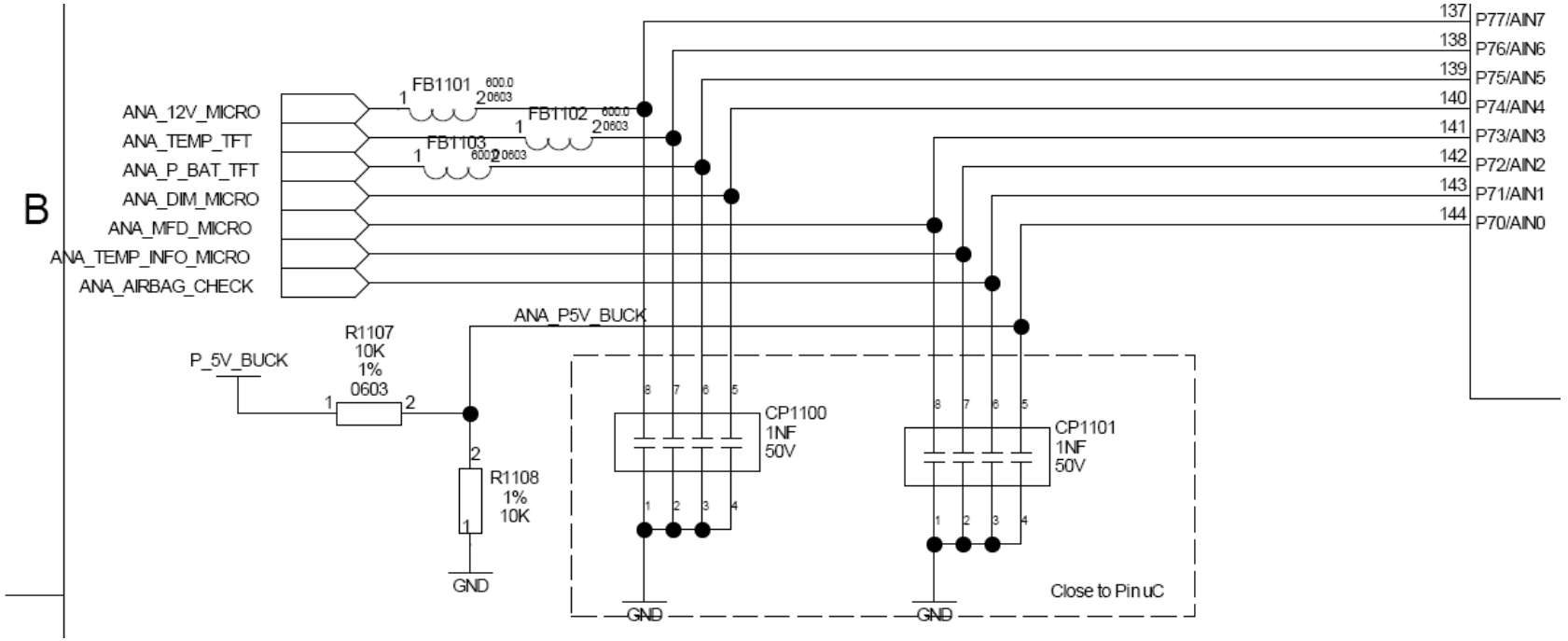
Avoid placing a series resistor on this line →

Series resistance makes the signal weak in the presence of interference



RF Immunity Countermeasures – ADC inputs I

- ADC inputs are particularly sensitive to RF interference
- Place one capacitor from line to ground and if line length is > ~ 7cm, provide 2 or more capacitors to prevent interference coupling
- A series ferrite may also be necessary if the problem is quite challenging:

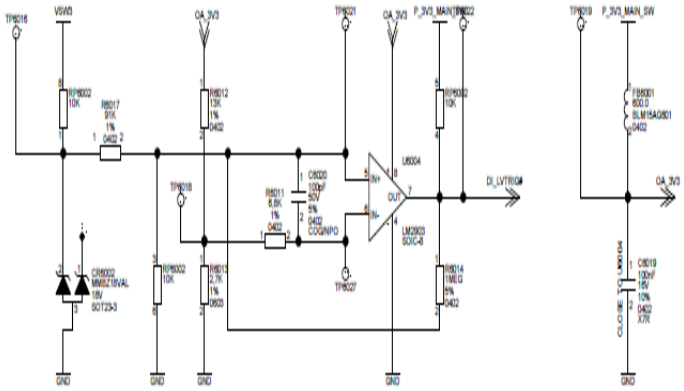


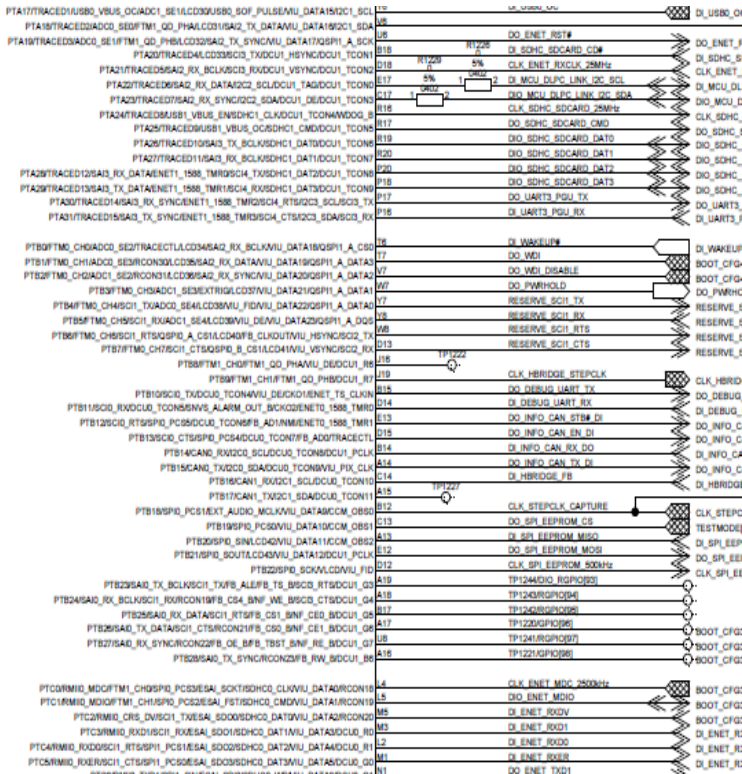
RF Immunity Countermeasures – ADC inputs II

- Not every EMC problem can be corrected at the HW level → always check the software acquisition algorithms on ADCs

- Warning!! Choosing capacitor values can have conflicting requirements!!
  - ADC stability requirements from HW point of view normally drive the value higher near 22nf
  - EMC requirements normally drive the value to be much lower (around 470pf or less) to prevent coupling at higher frequencies
  - A value of 1nf is a good compromise

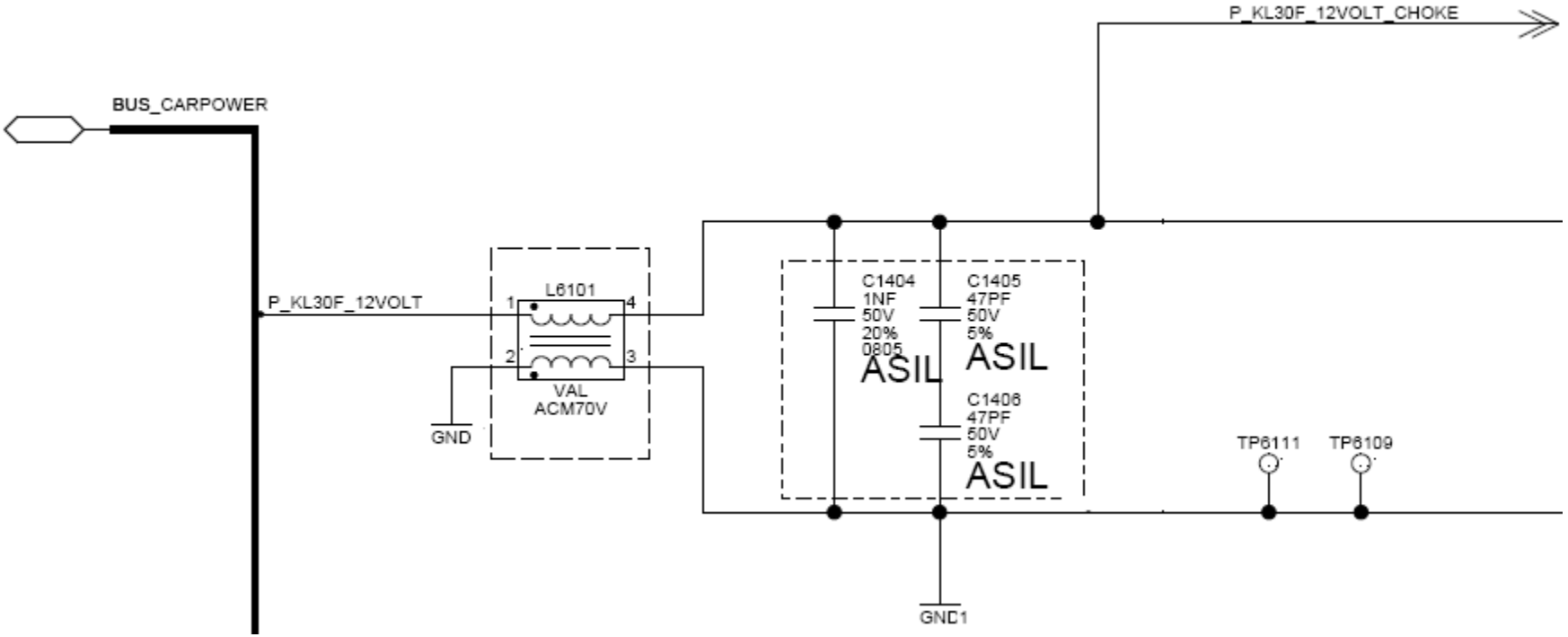
Shematic design – EMC overview Emissions



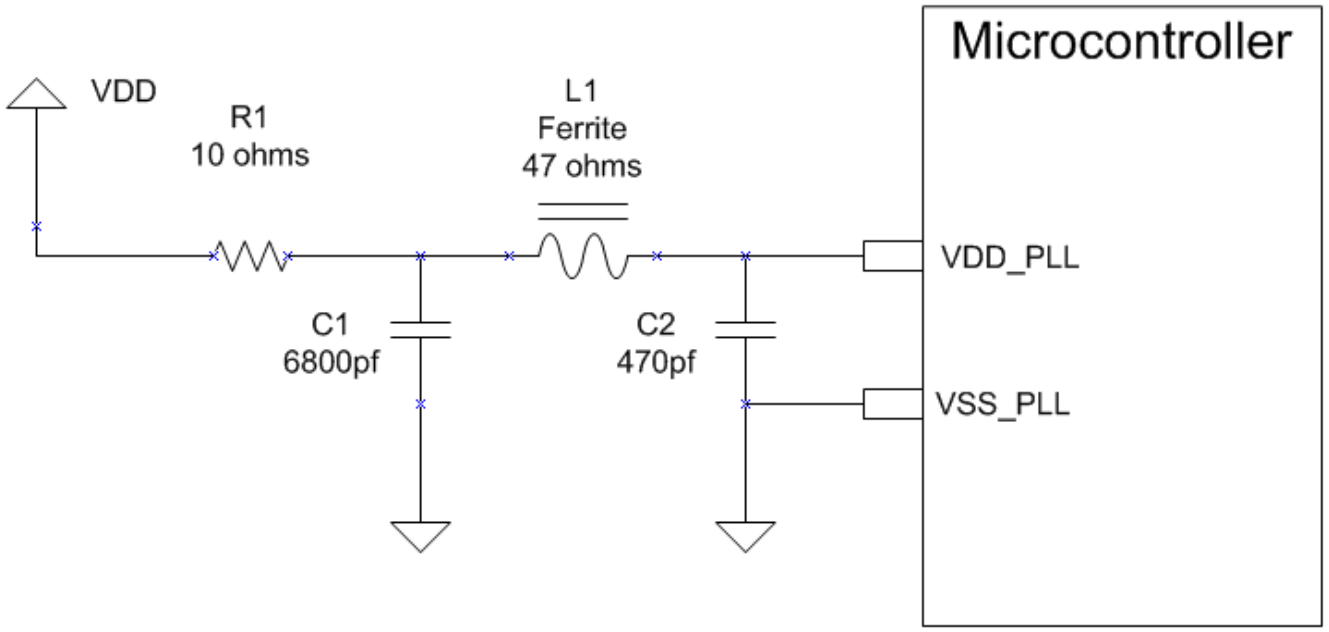


RF Emissions Countermeasures – SMPS Input CMC Filter

- Common-mode choke forces noise currents on both power and ground lines to be cancelled in a toroid shaped core or ferrite block core
- Circuit example: implemented on the front end power connections to product

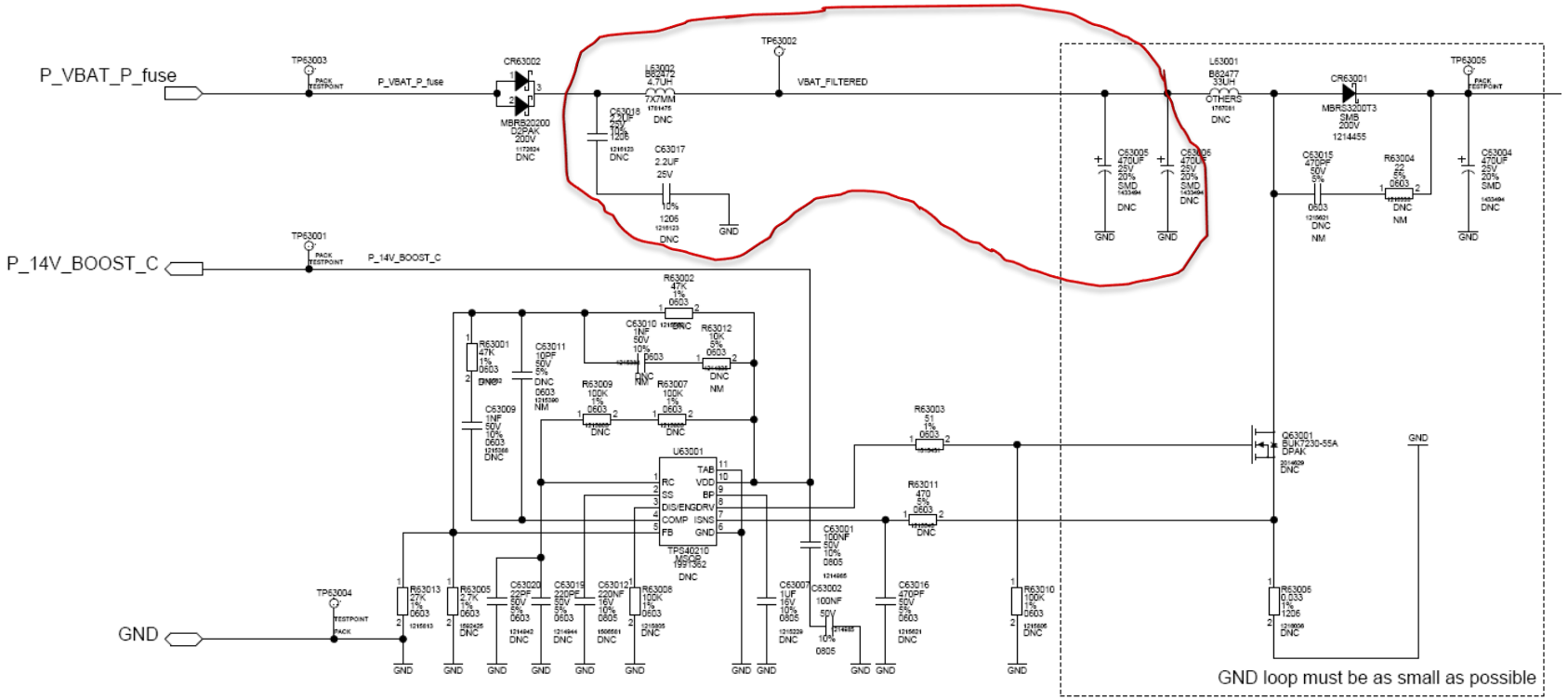


- By default, provide 1 capacitor for each power pin of the uC
- Start with 1nf and adapt the value to the expected harmonic content
- *For PLL pins*, provide a “PI” filter involving a low impedance ferrite component



RF Emissions Countermeasures – SMPS Input ‘PI’ Filter

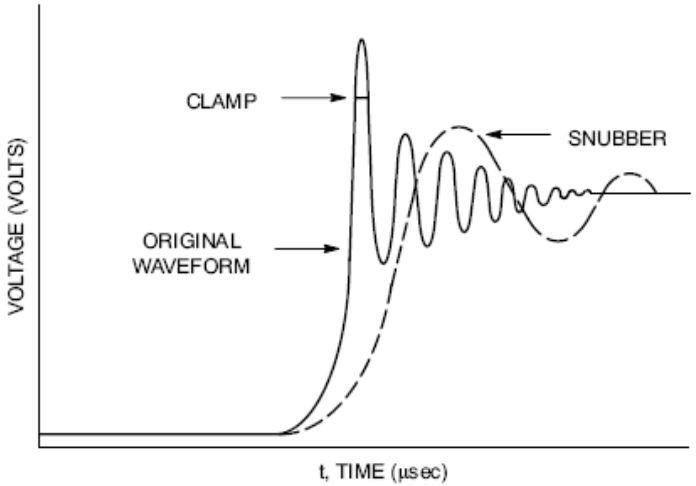
- Input filter “PI” filter is used to reduce dv/dt & di/dt on vehicle harness wires:



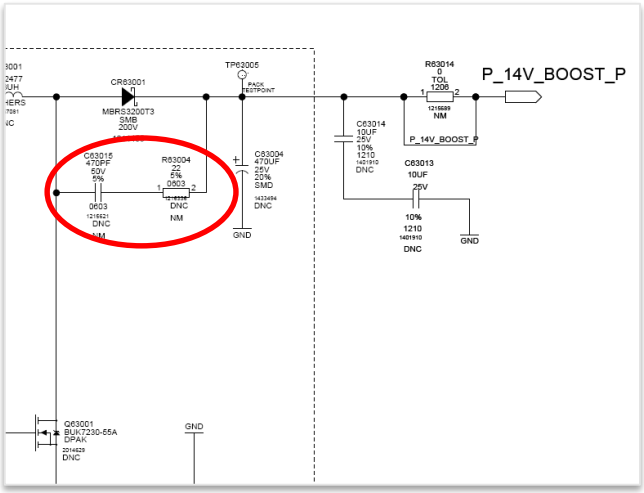
- Design cutoff frequency to be below fundamental switching frequency

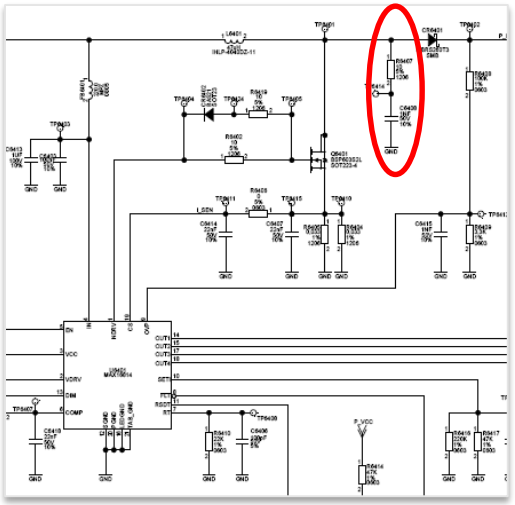
RF Emissions Countermeasures – SMPS Snubber Circuits

- Parallel snubber circuits are added to change switching characteristics
- Snubbers improve EMC, but cause power losses! ➔ Thermal issues?!
  - Include losses in efficiency calculation
  - Ensure snubber device(s) can sustain the power dissipation applied



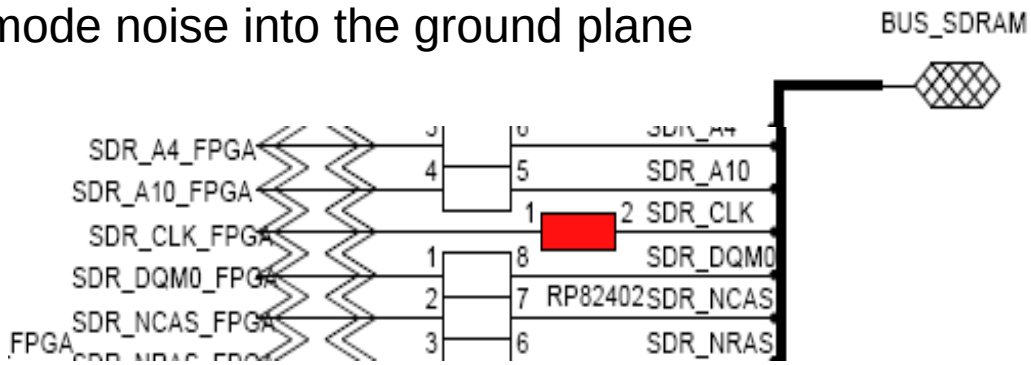
The Effects of a Snubber versus a Clamp





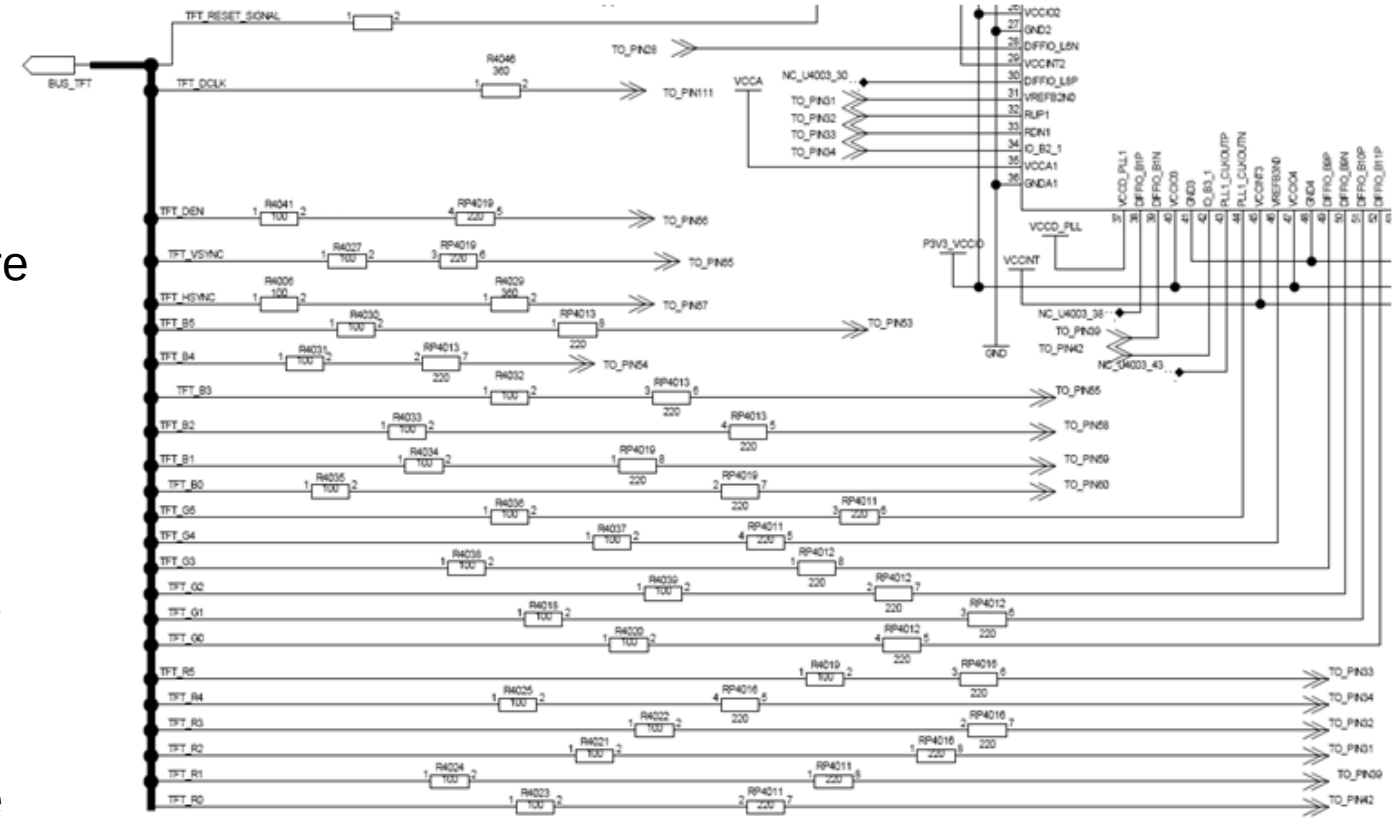
- FET bodies → RC snubber
- Inductors → CC snubber
- Diodes (boost & buck) → RC or just C snubber

- Provide a series termination component located near the driver
  - Goal is to reduce the current flowing in the trace to the load/receiver
  - Must maintain ‘proper’ waveform at receiver input
  - Resistor + Ferrite series combination used to achieve better harmonic noise reduction
- NOT recommended to add parallel capacitor to ground at the receiver
  - Good: This causes further ‘slewing’ of the waveform to reduce harmonics
  - Bad: Injects common mode noise into the ground plane



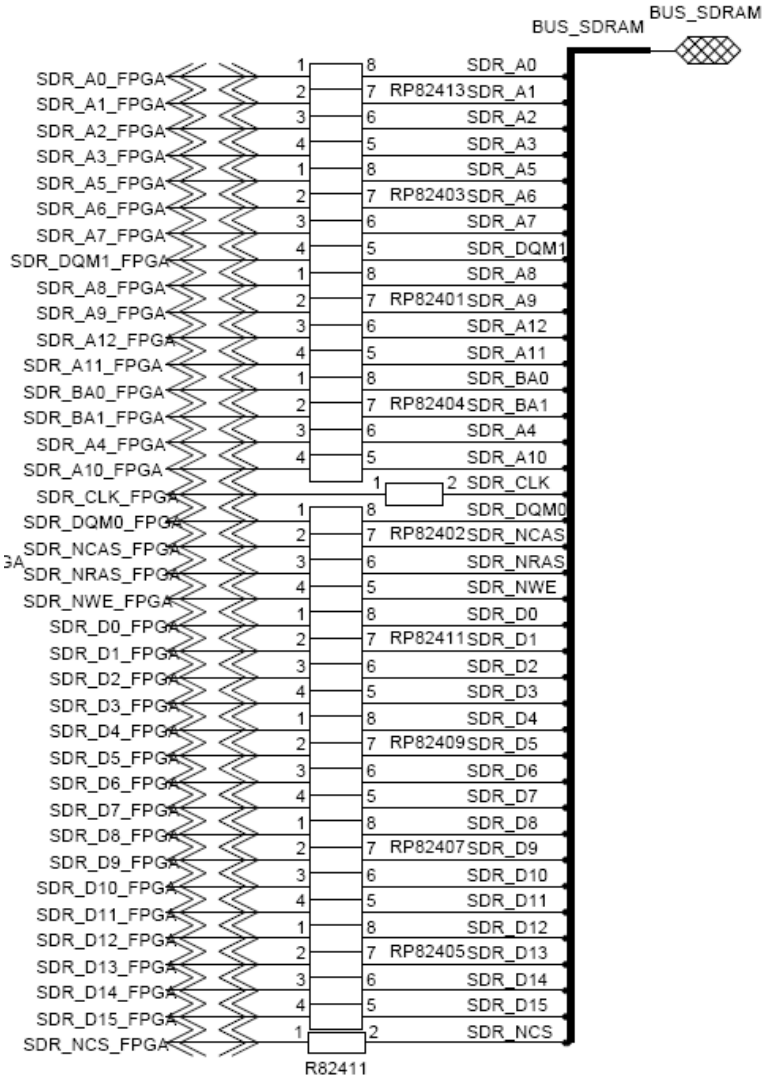
RF Emissions Countermeasures – TFT BUS

- Provide series terminations for all lines
- Keep in mind there may be multiple devices in parallel (eg. Flash + SDRAM)
- Termination value maybe limited by functional/timing requirements of the interface



RF Emissions Countermeasures – Memory BUS

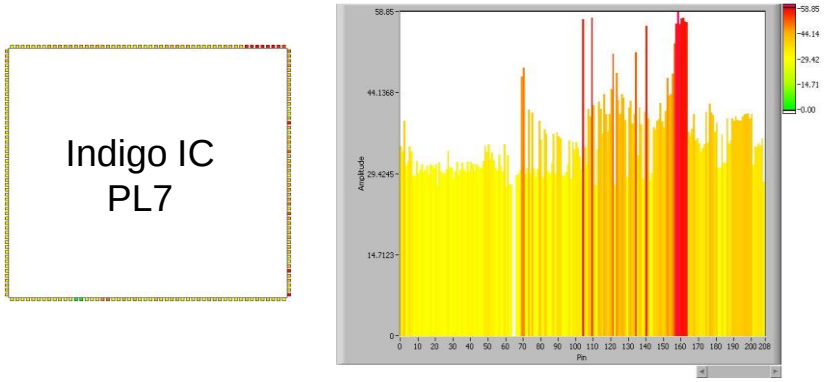
- Provide series terminations for all lines
- Keep in mind there may be multiple devices in parallel (eg. Flash + SDRAM)
- Termination value maybe limited by functional/timing requirements of the interface



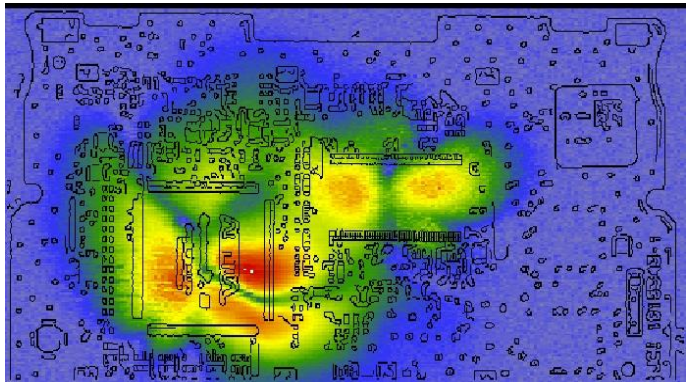
RF Emissions Countermeasures – Microcontrollers

- Emissions coming directly from a microcontroller are not easy to control!
  - Conducted noise from pins
  - Radiated noise from the die / lead frame
- Use IEC61967 EMC report for RE and CE performance of micros
  - Identify high emissions on IC pins, then add series filters on those pins
  - Identify high levels of radiation from IC, then add provision for EMC shield

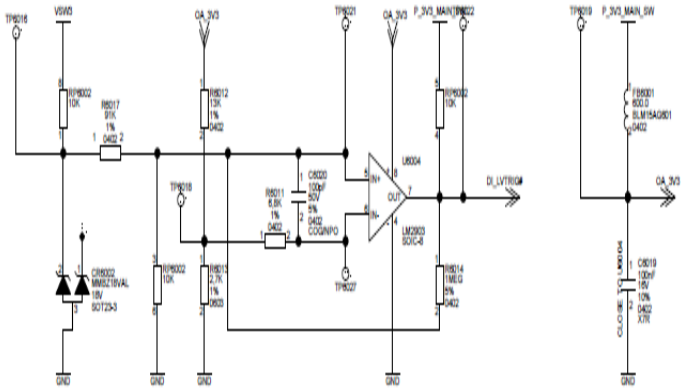
Pins Measurements @ Visteon

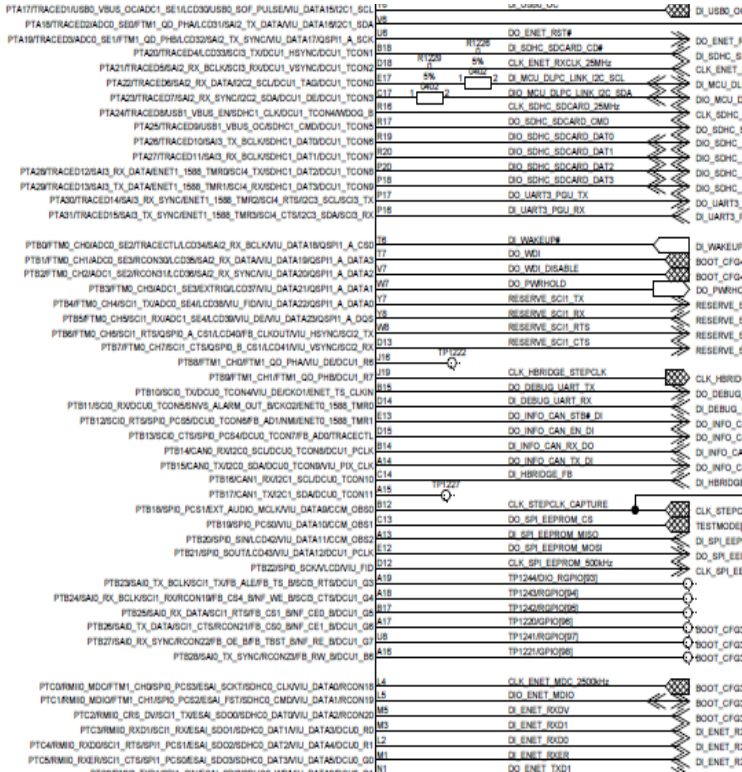


RF Scan @ Visteon



Shematic design – EMC overview ESD



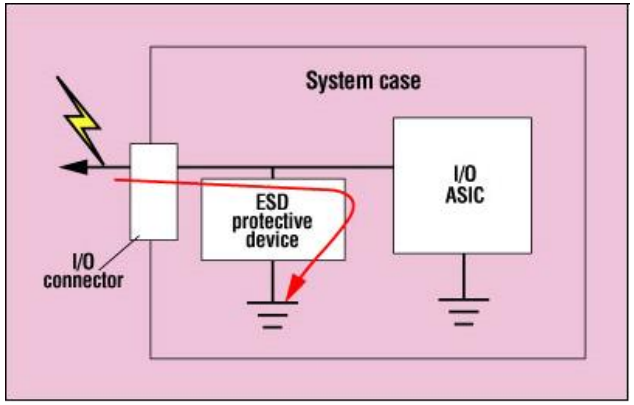


ESD Countermeasures – Overview

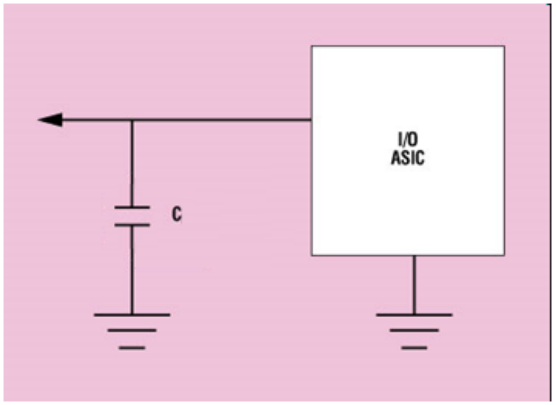
- Direct discharge is typically handled at the electrical HW design level
  - Vehicle connector pins, inputs and outputs
  - Audio jacks, antenna connections, USB cables
  - Don’t forget board to board connectors and flex cables!
- Air discharge is typically handled at the mechanical level of product design
  - Prevent open gaps around displays (use overlaps)
  - Minimize number of holes, vents and openings in housings
  - Increase the distance between openings and electronics parts inside

ESD Countermeasures – Direct Discharge

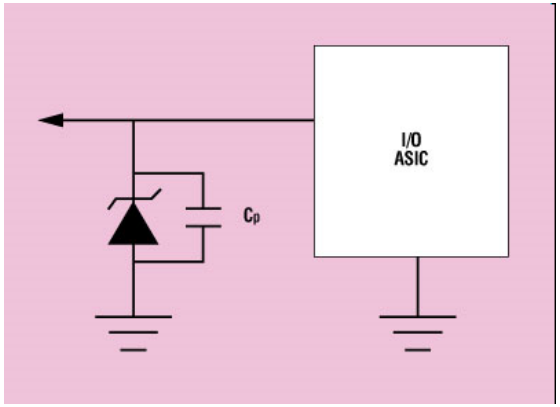
- **ESD Suppression:** ESD protection devices attempt to divert a potentially damaging charge away from sensitive circuitry and protect the system from permanent damage
- At the vehicle connector a 0.01uf capacitor can be placed between the line and ground



System Overview



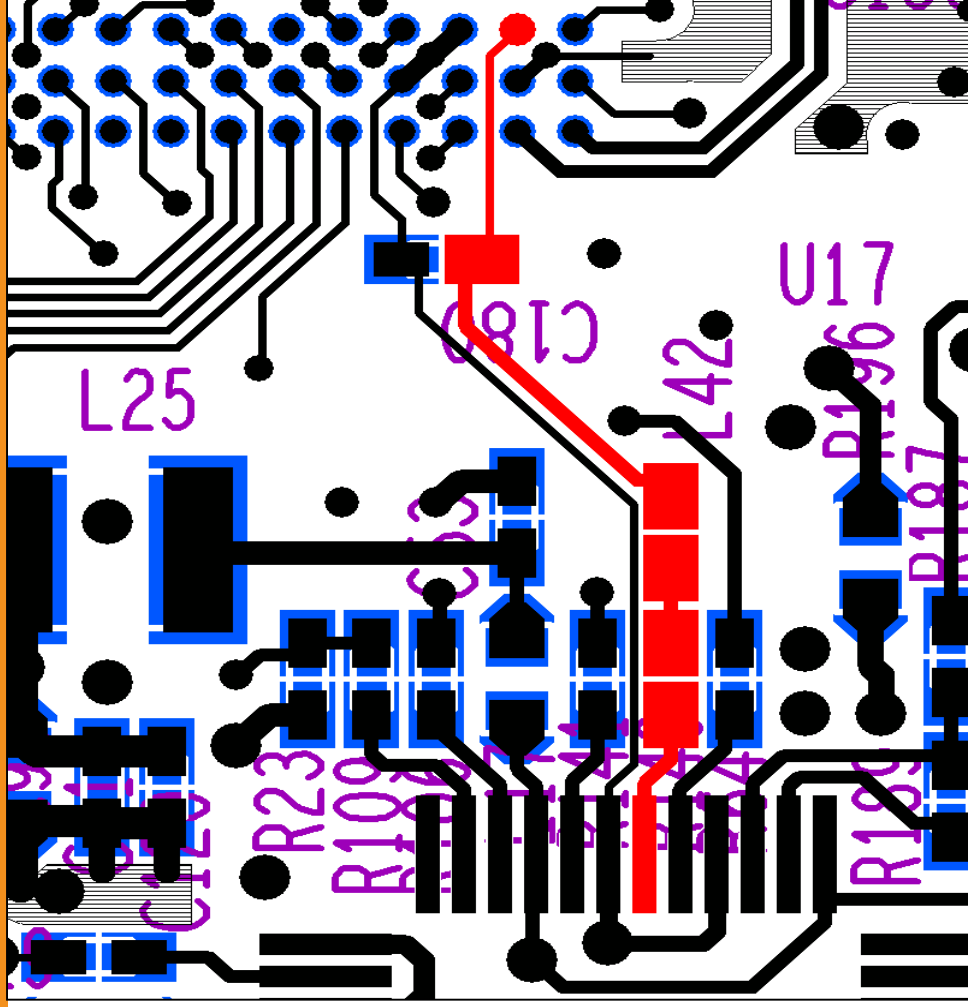
Default Signal Protection

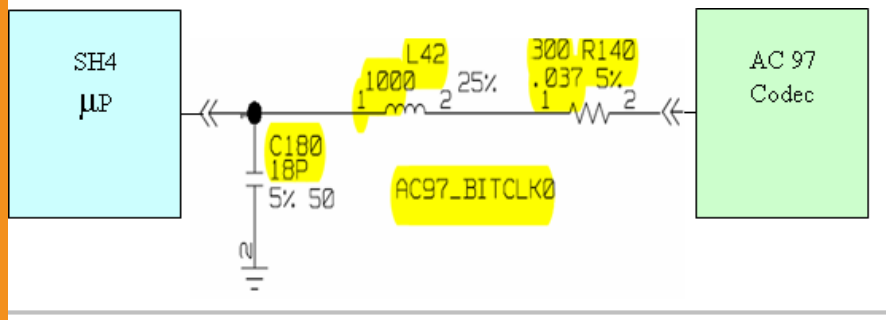


Alternative Signal Protection

- Sometimes capacitors can add too much capacitance on the line for the function to operate correctly (eg. CAN, LIN, APIX, LVDS, etc..)
- Alternatively use low capacitance clamping diodes

Slew Rate Control

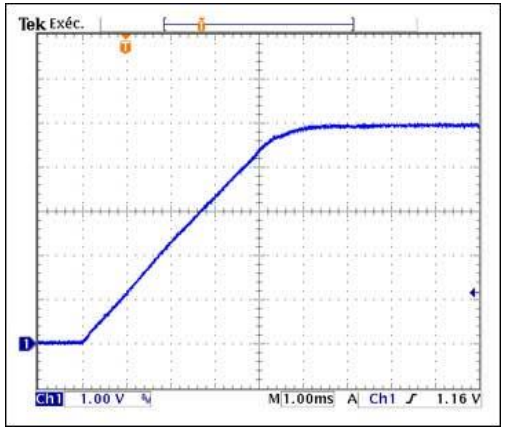




What Does ‘Slew Rate’ Mean?

- *Definition:* Amount of voltage/current rise divided by the change in time

5 Volts



5 ms

$\Delta V = 5\ V$

$\Delta T = 5\ ms$

$\Delta V/\Delta T = 1V/ms$

Also referred to as:
dV/dt or dI/dt

How do Slew Rate Controls Work?

–R-L-C slew rate controls

- Reduce current flowing in the line
- Increase time constant
- Inductor current cannot change instantly
- Capacitor voltage cannot change instantly

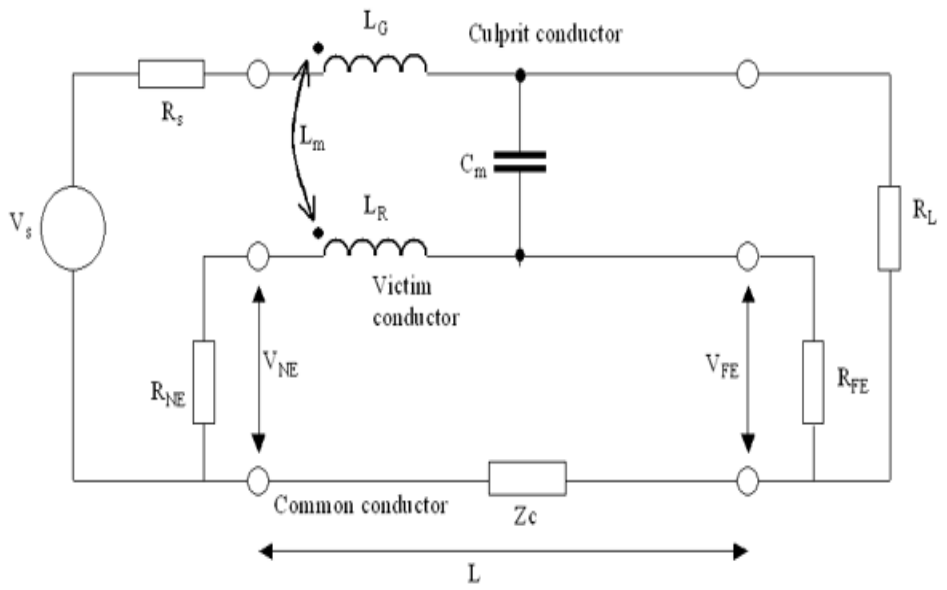
–Gate drive bias control

- Controlling the rate at which gate capacitance is charged on a FET
- Controlling the current flow into the base on a BJT

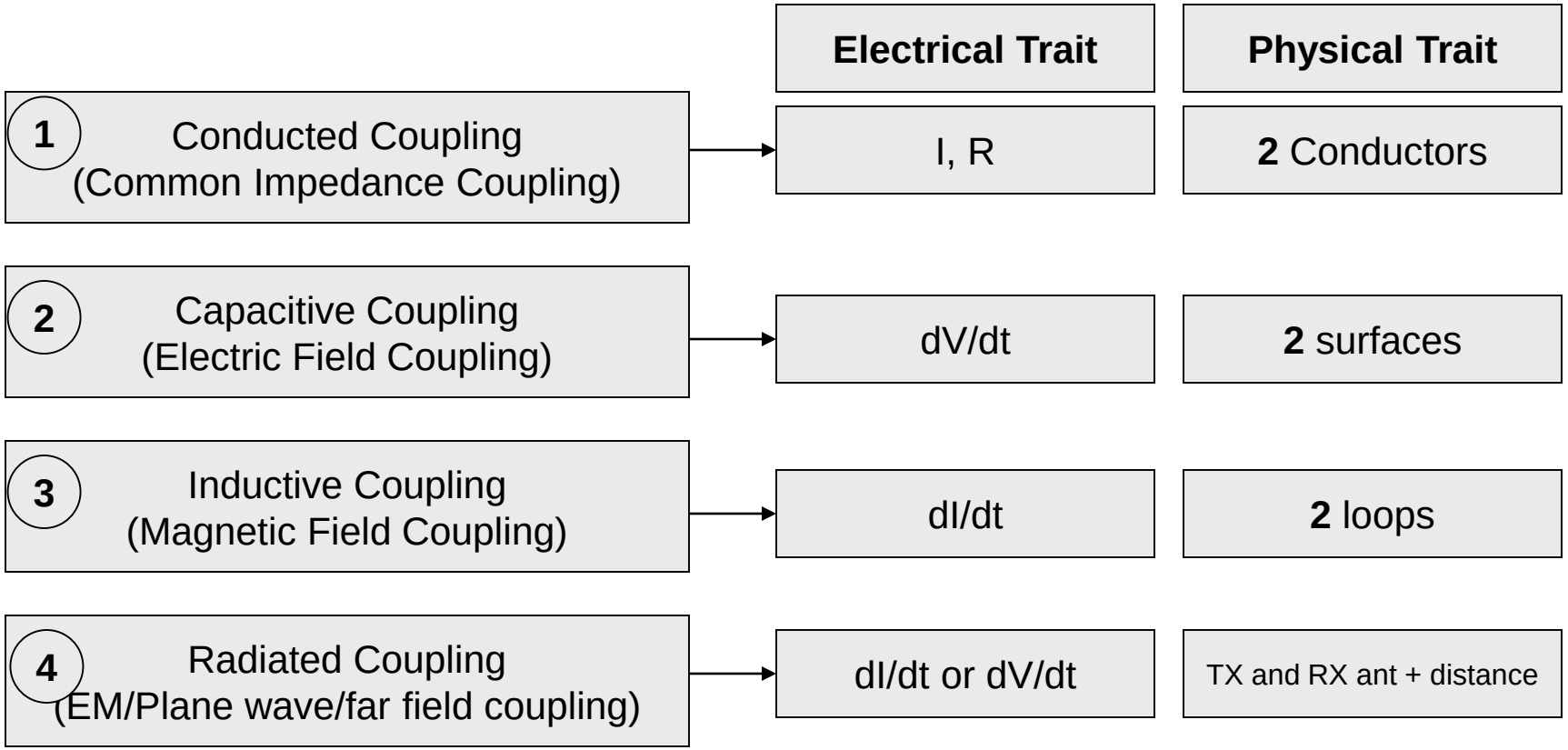
Place series component near the driver!

Place parallel components near the receiver!

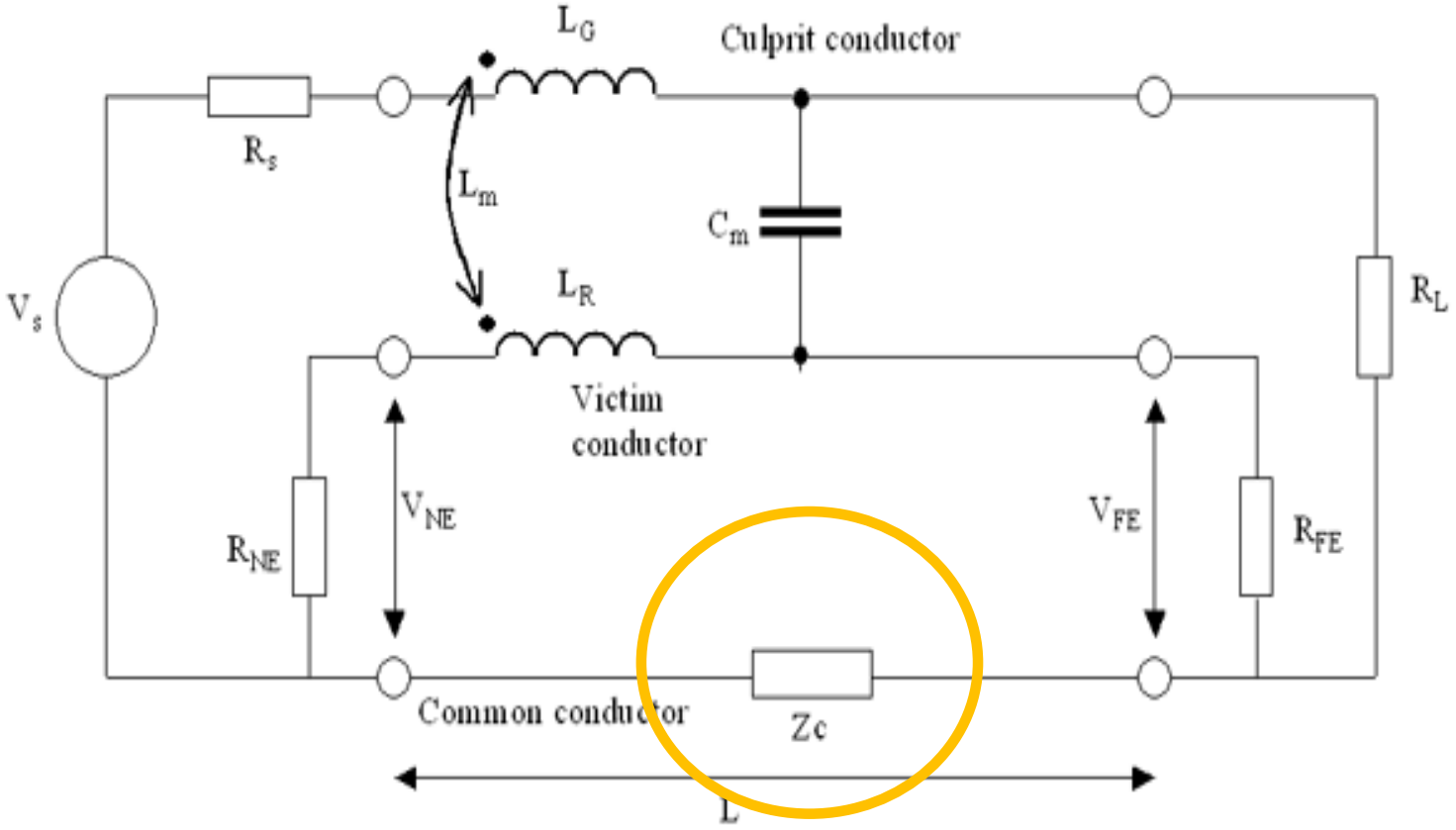
Coupling Mechanisms



Coupling Mechanisms

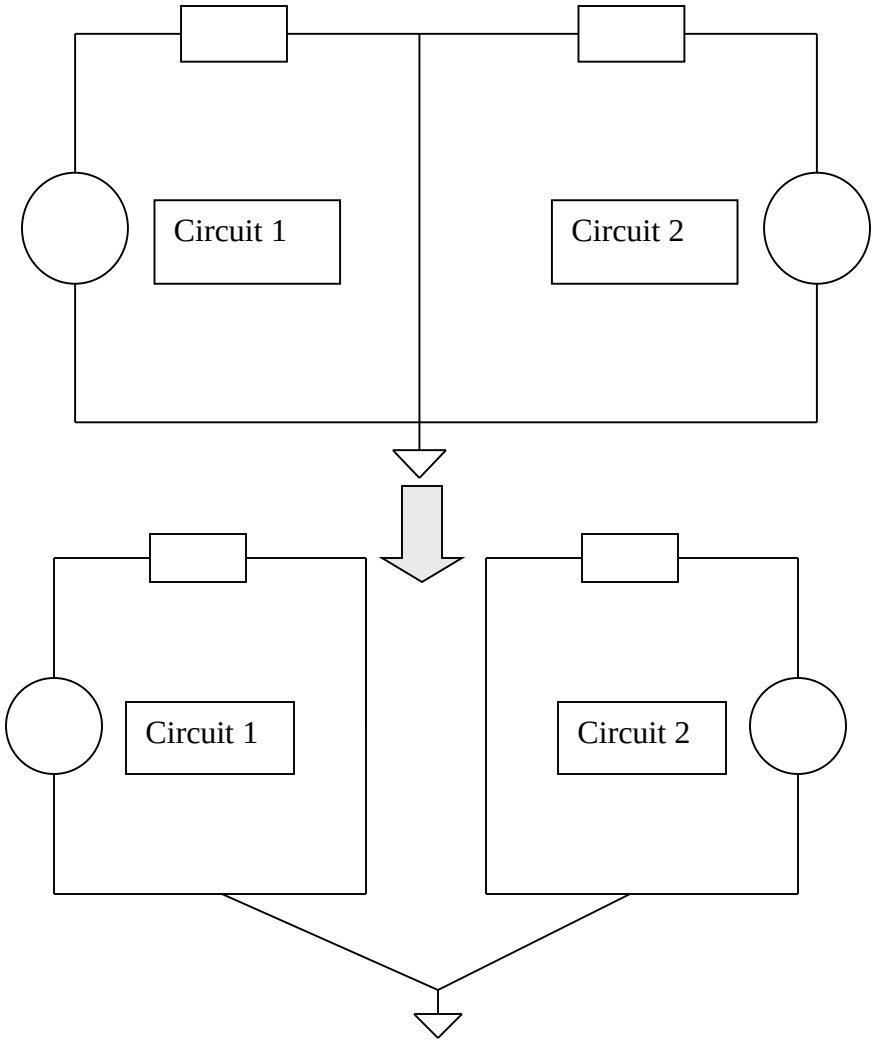


Common Impedance Coupling

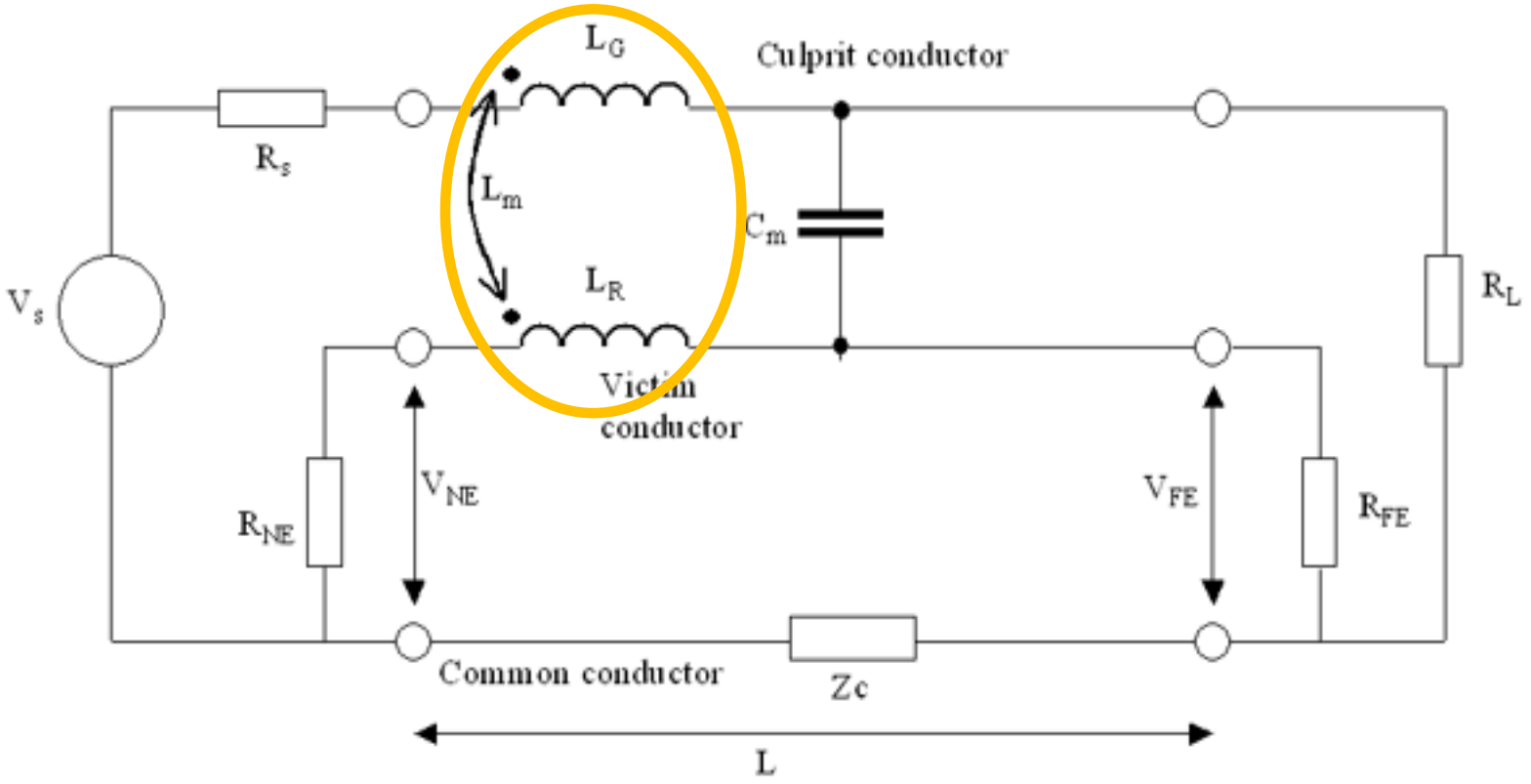


Common Impedance Coupling Mitigation

- Filter conducted noise
- Remove common path

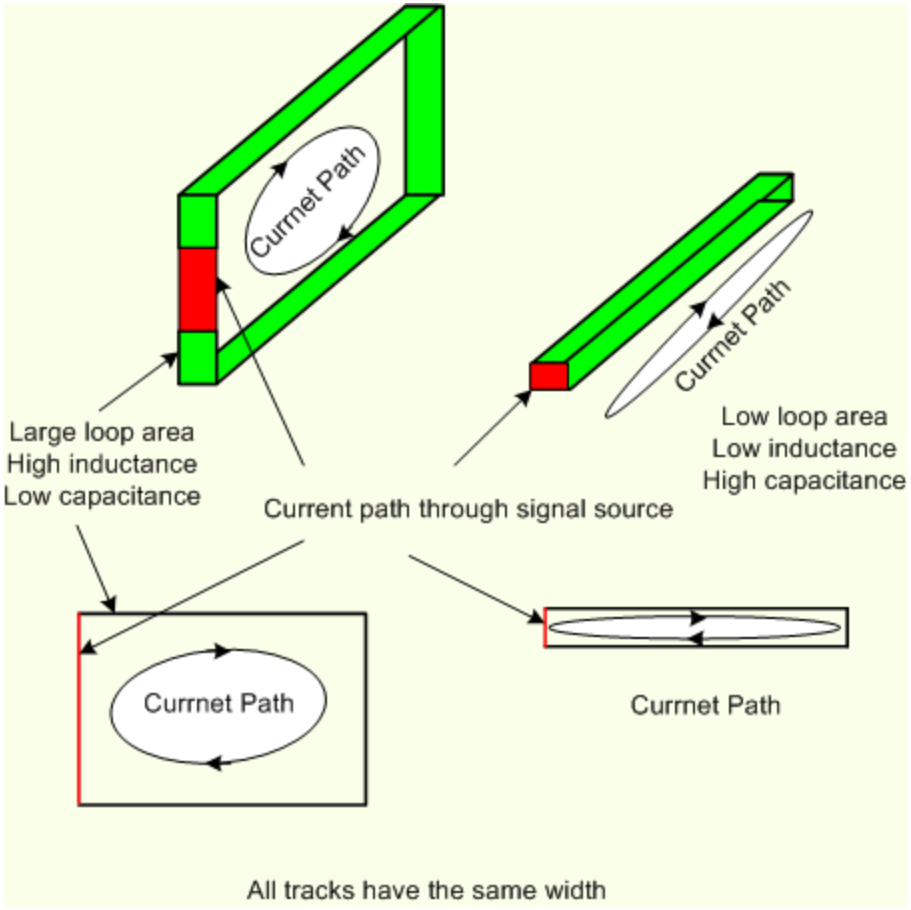


Inductive Coupling



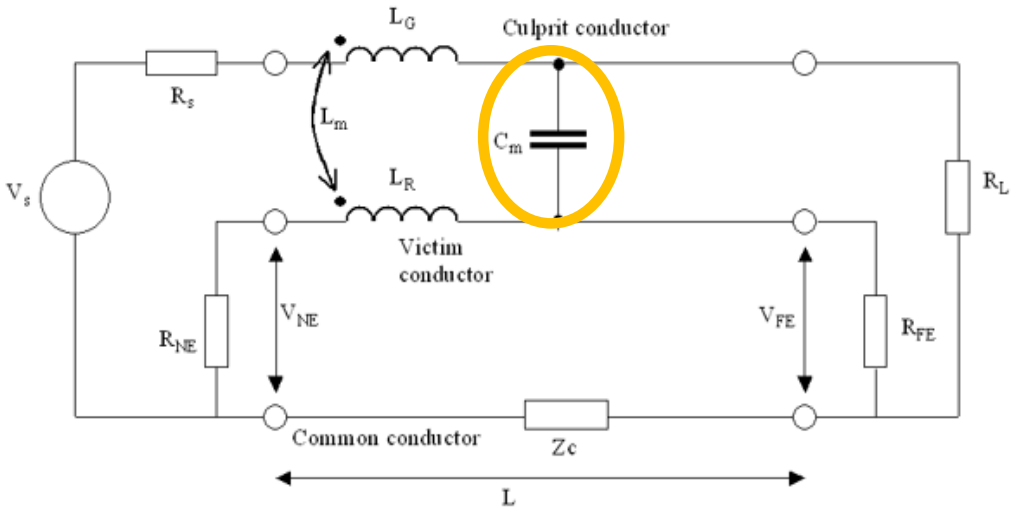
Inductive Coupling Mitigation

- Increase R(load) relative to R(source)
- Decrease loop areas
- Bring return plane closer



Capacitive Coupling Mitigation

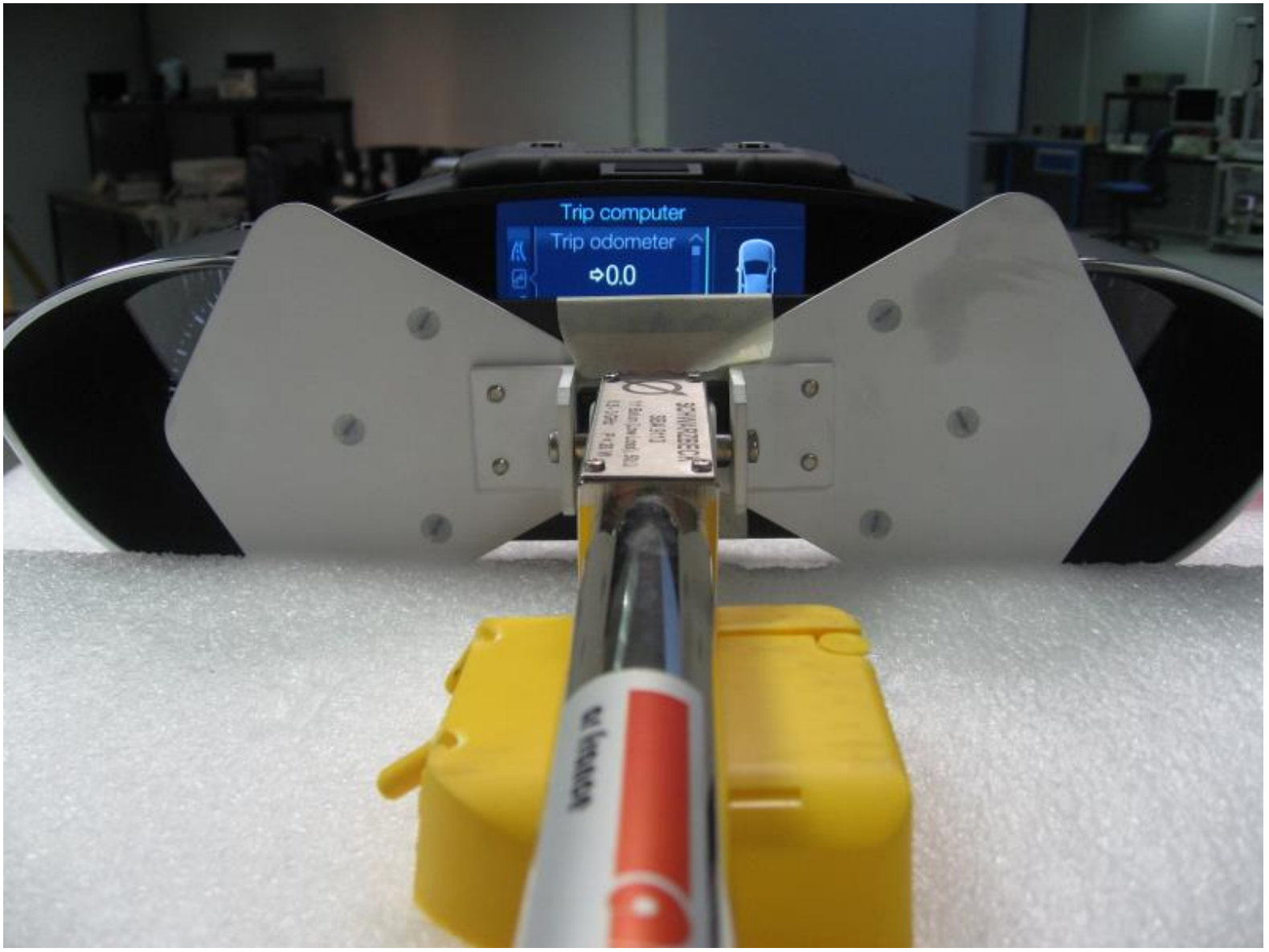
- Increase distance between circuits
- Reduced surface areas of copper
- Field containment
- Divert noise current by using shield
- Use guard trace



• High impedance inputs (operational amplifier) are very sensitive to external noise → Keep Short Traces

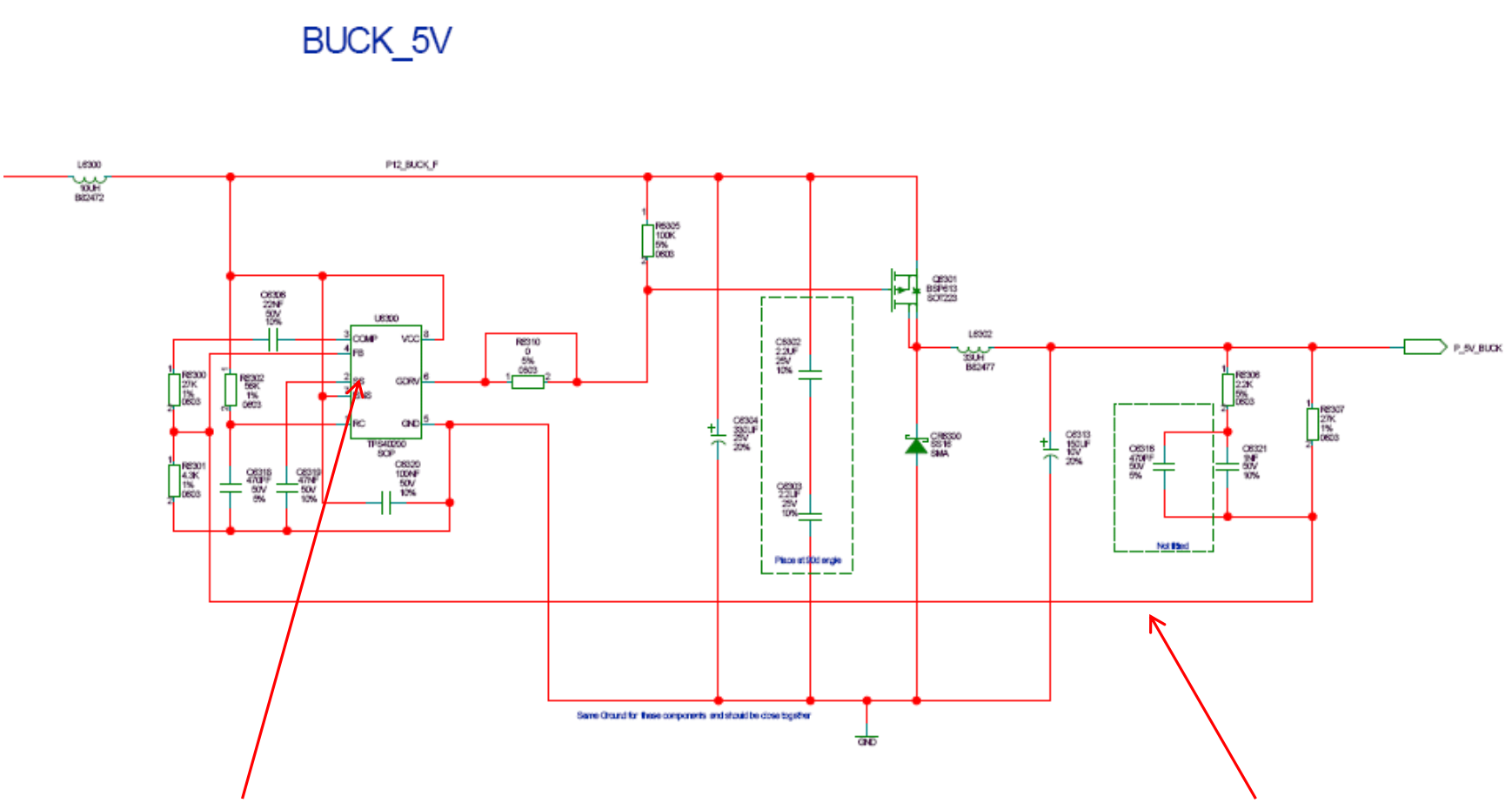
Capacitive Coupling Example: Immunity

Ford Cluster – 5V Buck Issue



Capacitive Coupling Example: Immunity

Ford Cluster – 5V Buck Issue



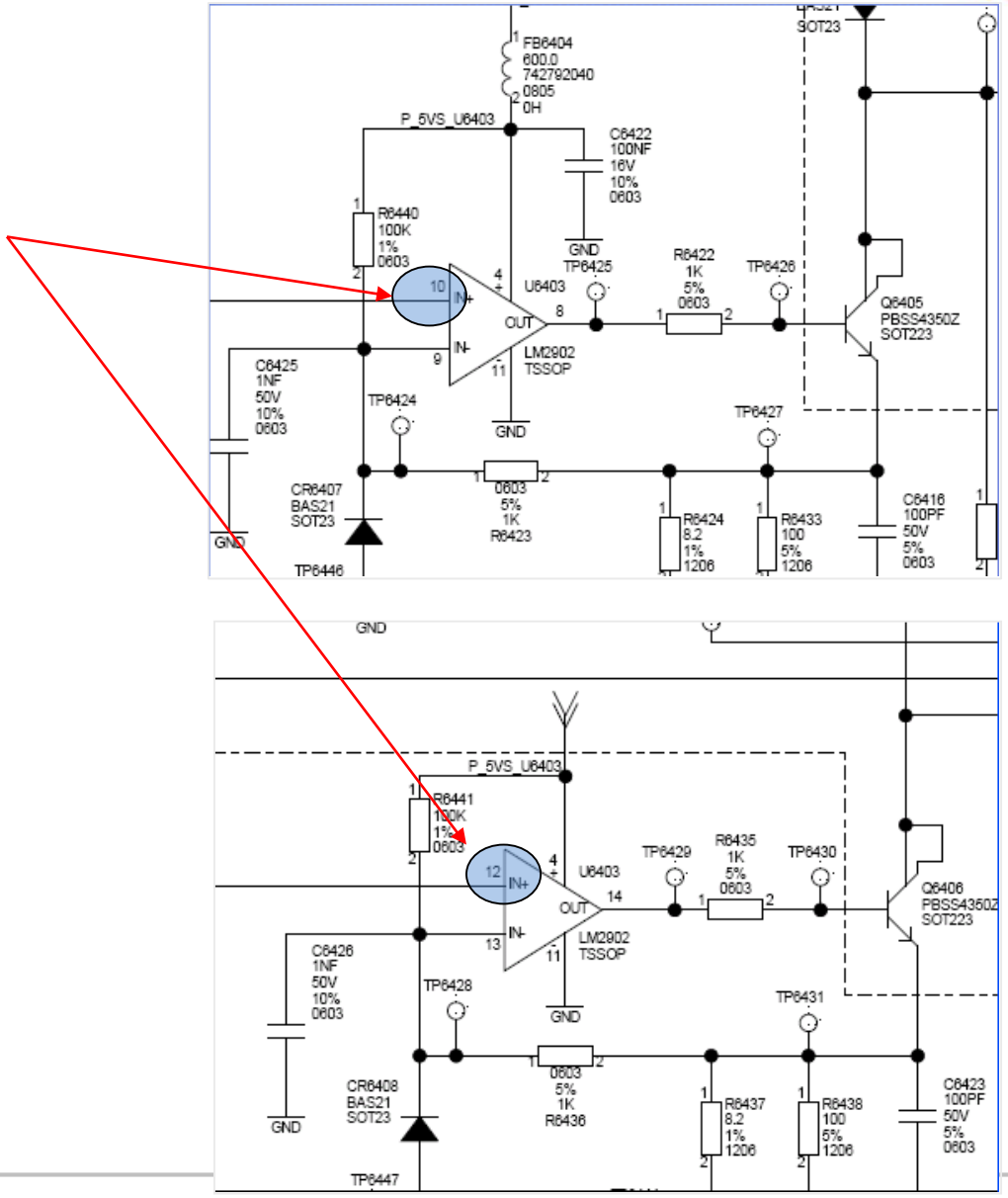
High impedance op-amp inside regulator
IC: no protection cap between inputs

Long feedback line

Capacitive Coupling Example: Immunity

BMW Cluster Backlighting Pulsing Issue On Vehicle

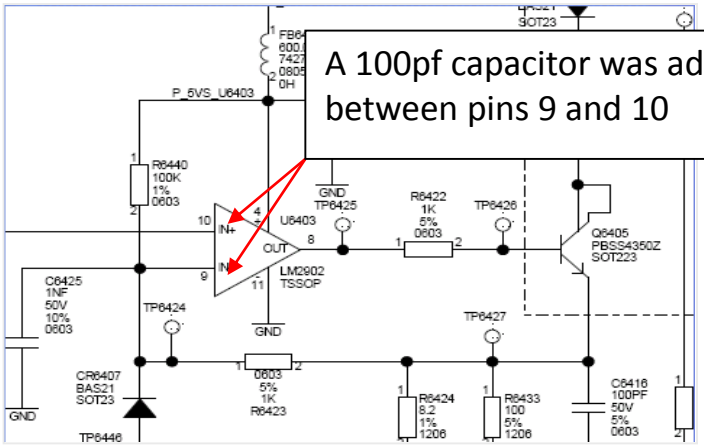
- Weakest points
  - Op-amp inputs pins 10 & 12 of U6403 IC

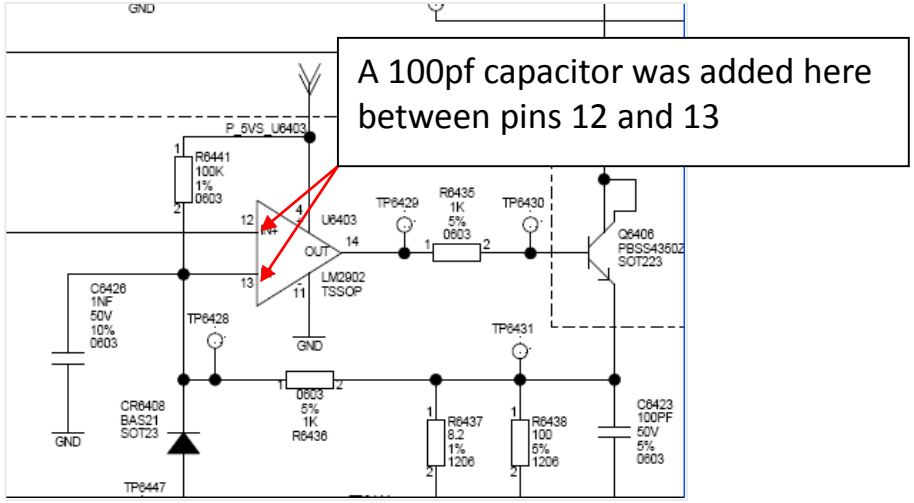


Capacitive Coupling Example: Immunity

BMW Cluster Backlighting Pulsing Issue On Vehicle

- Improvements made
  - Add 100pf capacitors to both op-amp inputs
  - All traces leading up to op-amp input lines reduced length, area and vias
  - Moved voltage divider circuit close to op-amp inputs
- RF level increased from 2.5Watts of near-field radiation to 9Watts
- BCI and vehicle level became full pass

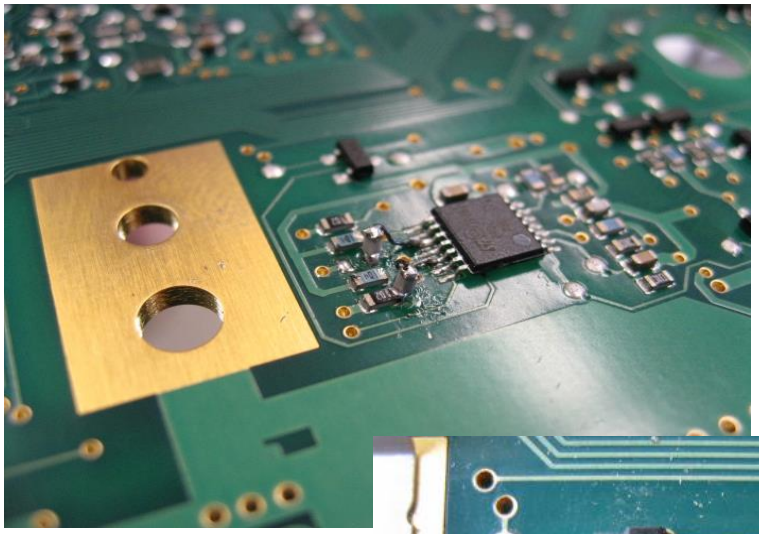




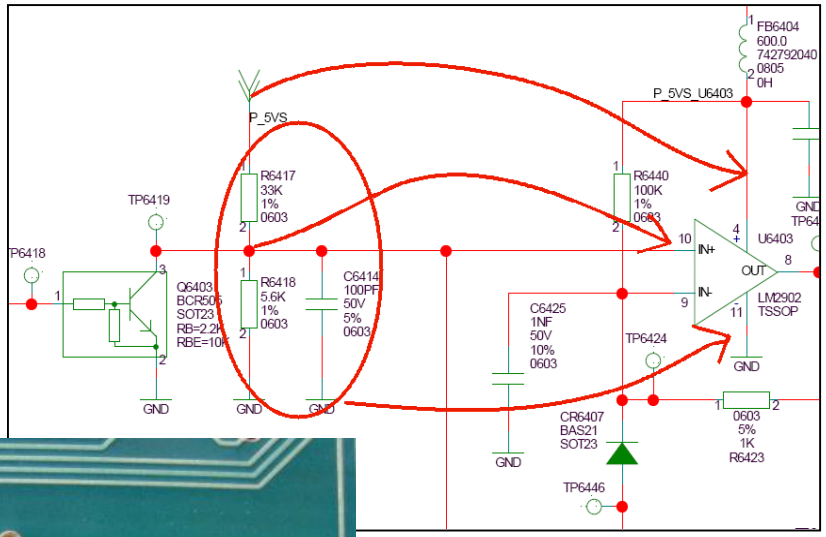
Capacitive Coupling Example: Immunity

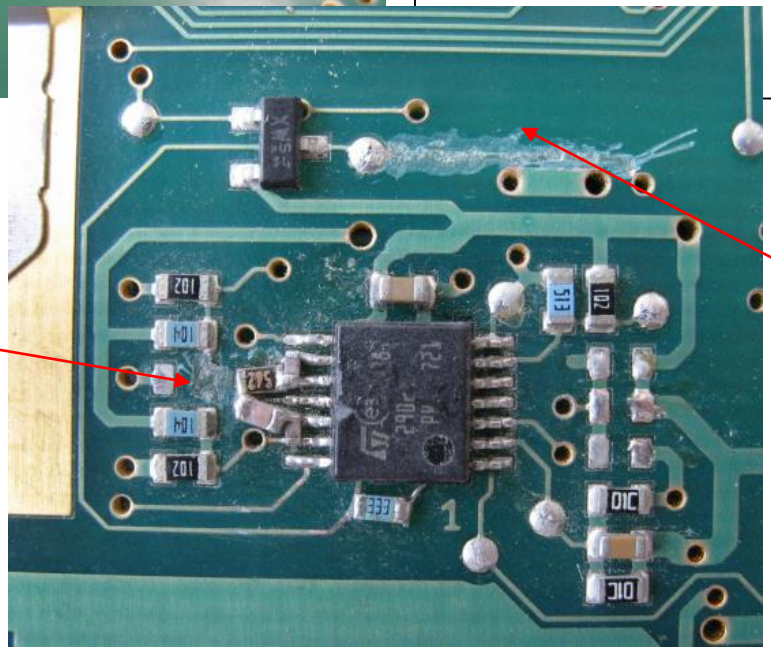
BMW Cluster Backlighting Pulsing Issue On Vehicle

Op-amp capacitors added



Voltage divider moved closer





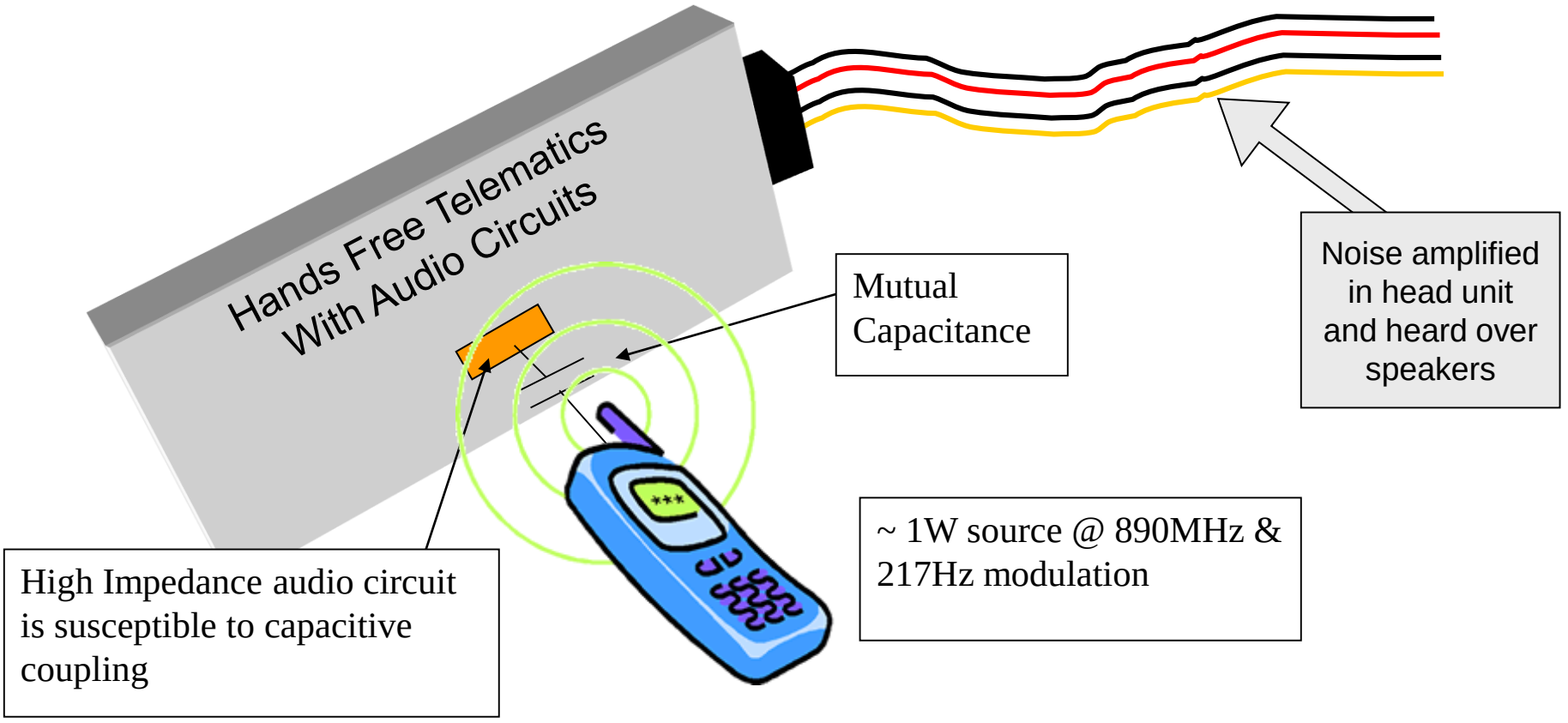
Voltage divider moved

Removed added trace length on op-amp inputs

Capacitive Coupling Example: Immunity

GSM Interference on HFT – Problem Statement

- **GSM** signal is capacitive coupled and demodulated to audio frequencies and passed into the audio system in the vehicle



Capacitive Coupling Example: Immunity

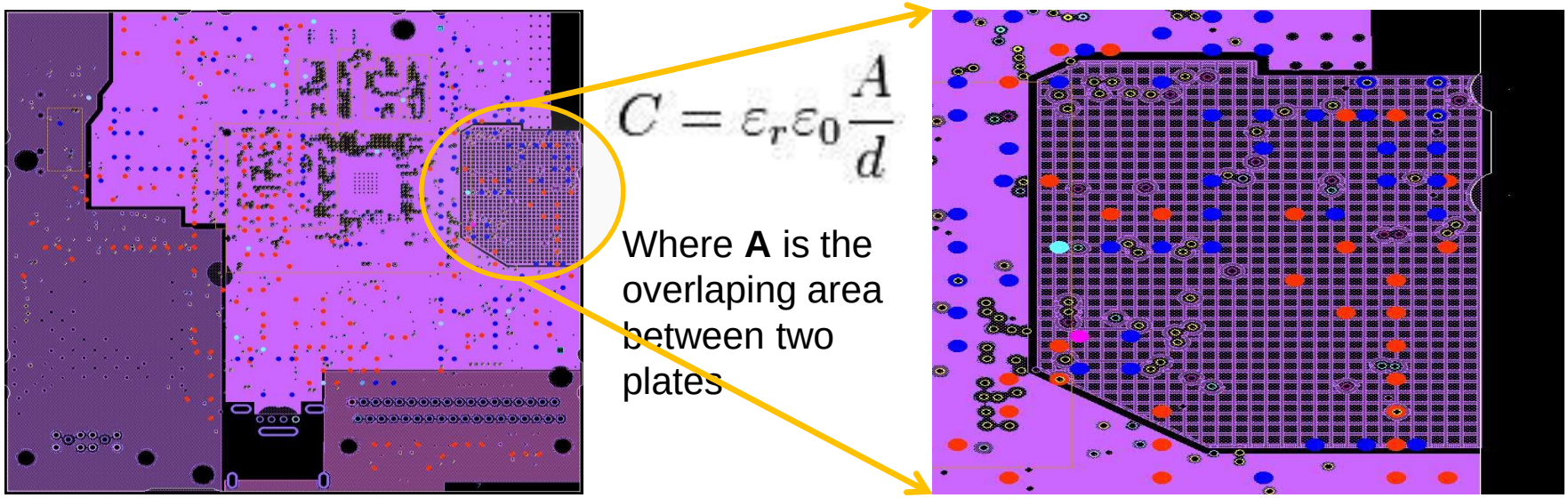
GSM Interference on HFT – Layout Changes Improve Immunity

–Audio circuit is connected to operational amplifier (inputs: AGND and Audio signal)

–AGND and Audio net acted as capacitive coupling ‘antenna’

–Improved Layout

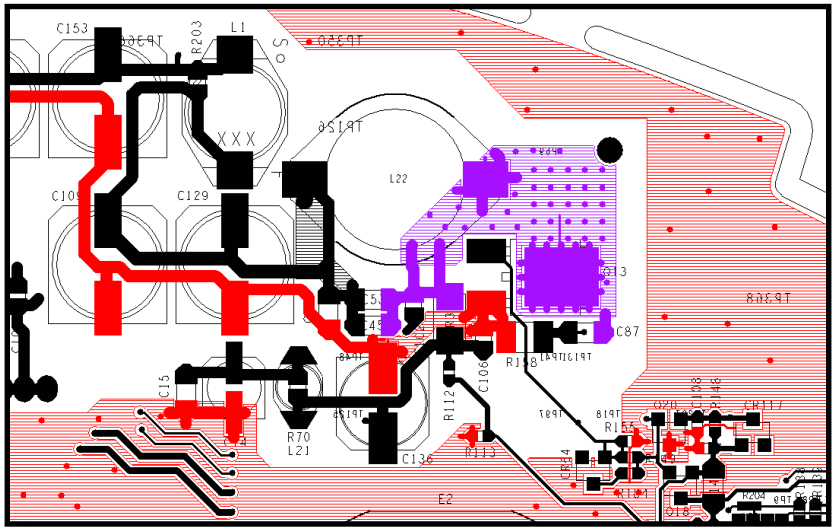
- Reduced copper area connected to AGND (analog ground)
- Made AGND ‘mesh area’ instead of filled copper
- Added by-pass capacitor directly at the input to op-amp between AGND and Audio Net



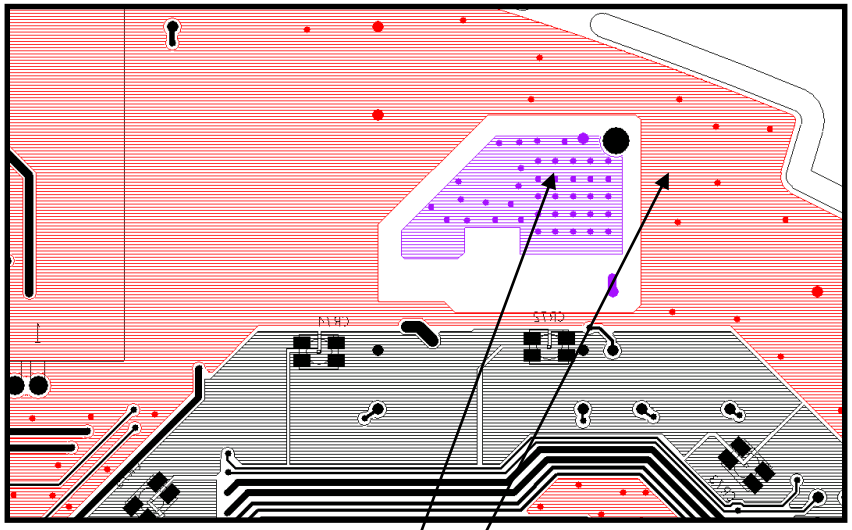
Capacitive Coupling Example: Emissions

Cluster – Boost Power Supply

TOP



BOTTOM



$$C_A := \varepsilon \cdot \frac{A}{D} \rightarrow 1.72pF$$

- 2 surfaces separated by a distance have capacitance
- A noise voltage in one metal object with respect to the other causes common-mode current to flow

- C = capacitance between switch node and ground
- E = permittivity of dielectric (~ 42 pF/m)
- A = square area of surface overlap (meters^2)
- D = separation distance (meters)

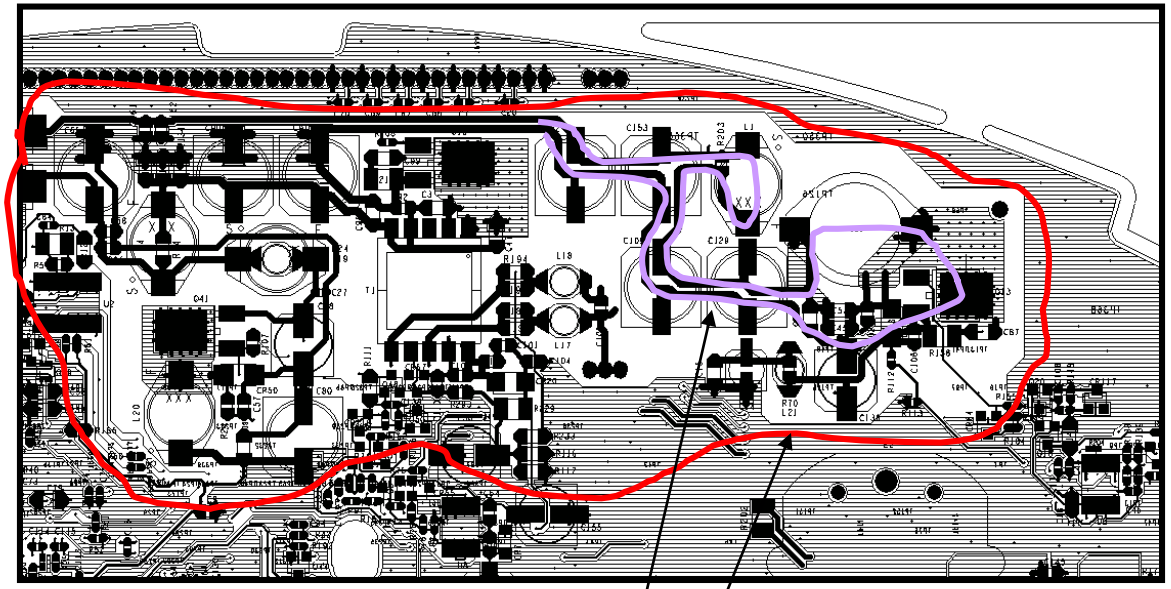
→ dV/dt

2 surfaces

Inductive Coupling Example: Emissions

Cluster – Boost Power Supply

Noisy loop
Ground loop



- Each loop has a self inductance (calculated)
- Mutual inductance forms between two overlapping loops

$$L_m := \sqrt{L_1 \cdot L_2} \cdot K$$

  - L_m = mutual inductance
  - L_1 = Loop 1 self inductance
  - L_2 = Loop 2 self inductance
  - K = coupling factor

$$L_{rect} = N^2 \frac{\mu_0 \mu_r}{\pi} \left[-2(w+h) + 2\sqrt{h^2+w^2} - h \ln\left(\frac{h+\sqrt{h^2+w^2}}{w} \right) - w \ln\left(\frac{w+\sqrt{h^2+w^2}}{h} \right) + h \ln\left(\frac{2h}{a} \right) + w \ln\left(\frac{2w}{a} \right) \right]$$

- RF current flowing in the noisy loop can produce a common mode voltage in the second loop
  - L1 = 50nH
  - L2 = 270nH
  - K = 0.45 (represents poor coupling between loops; where 1 = perfect coupling)

- L_m = 52nH → mutual inductance between loops

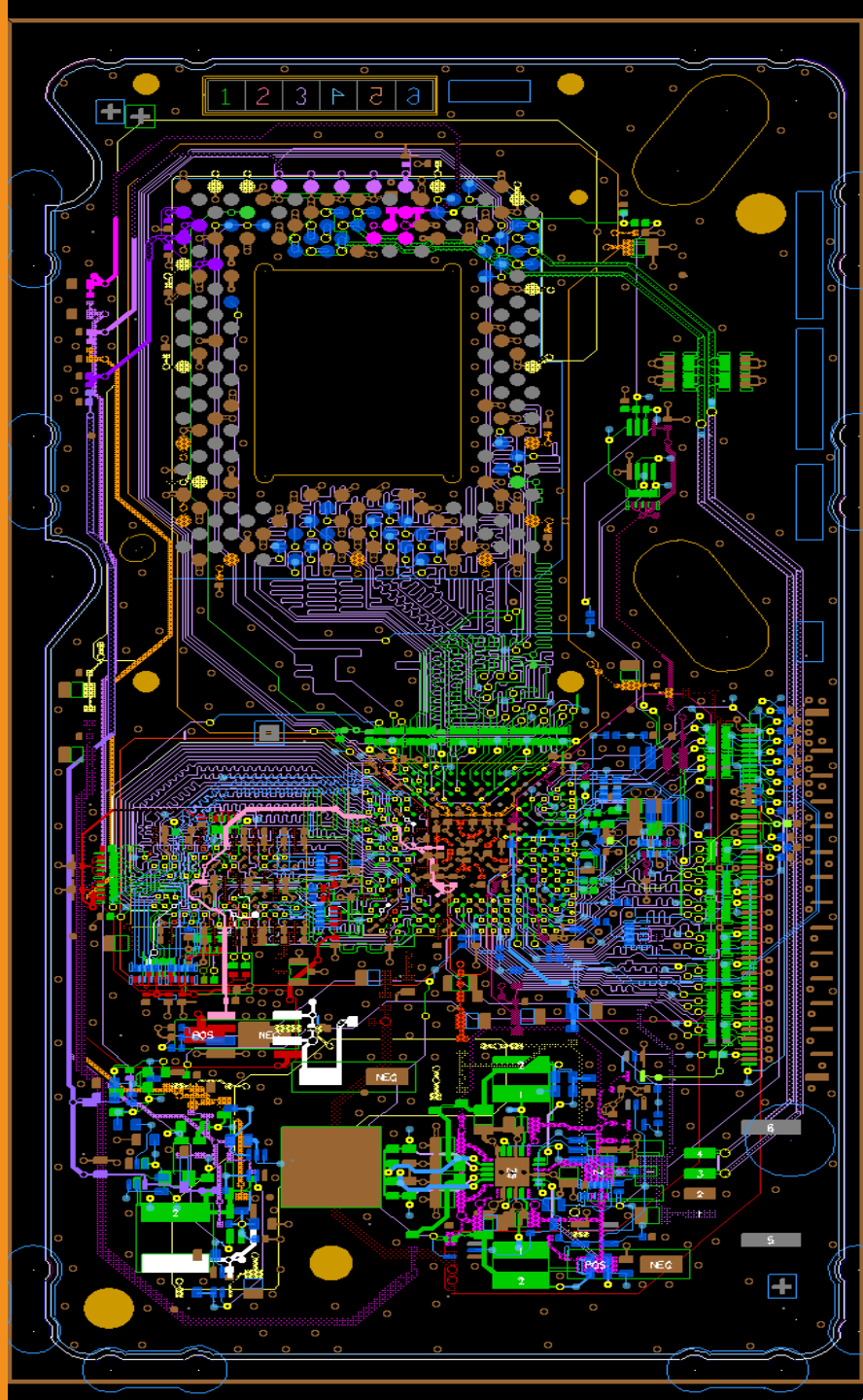
→ dI/dt | **2** loops

EMC Guidelines Summary

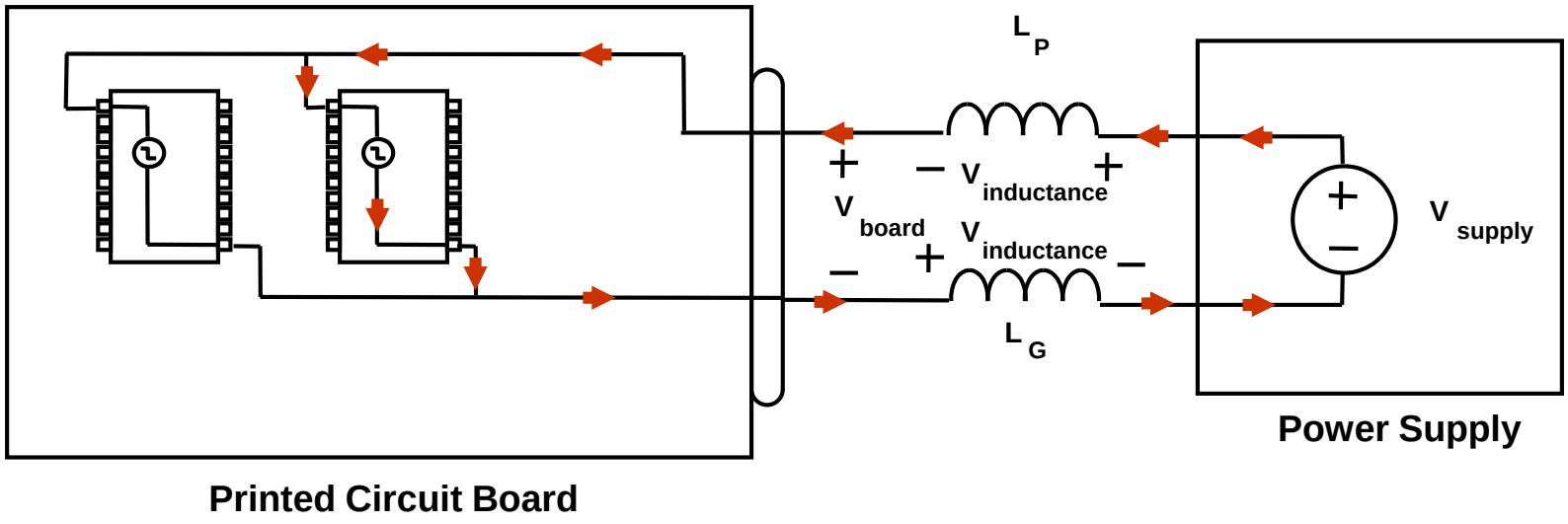
How to reduce coupling problems

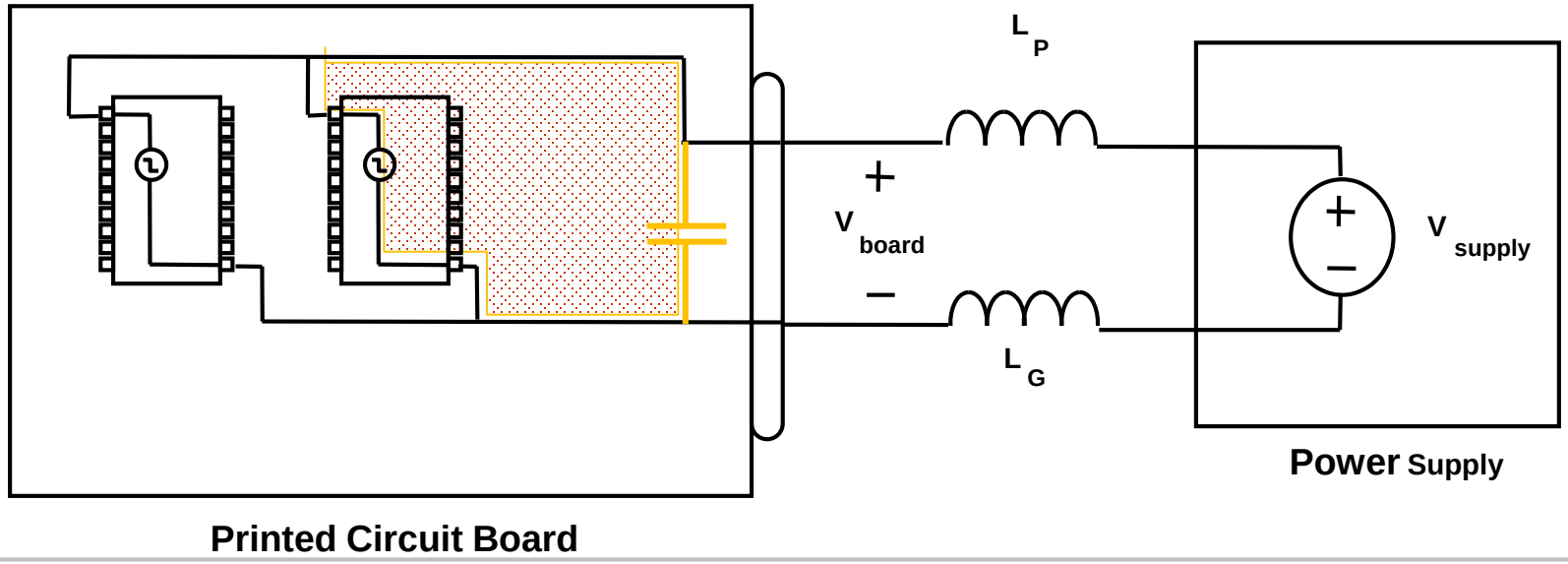
- Path → Capacitive Coupling
  - Increase separation of two metal surfaces
  - Reduce area of overlap between metal objects
  - Reduce rate of change for voltage (dv/dt)
- Path → Inductive Coupling
  - Decrease loop areas
  - Reduce rate of change for current (di/dt)
  - Create poor coupling between source and victim loops (reduce K)
- Path → Radiated Coupling
  - Reduce loop size and longest dimension
  - Increase distance between source and receive

PCB Layout – EMC overview

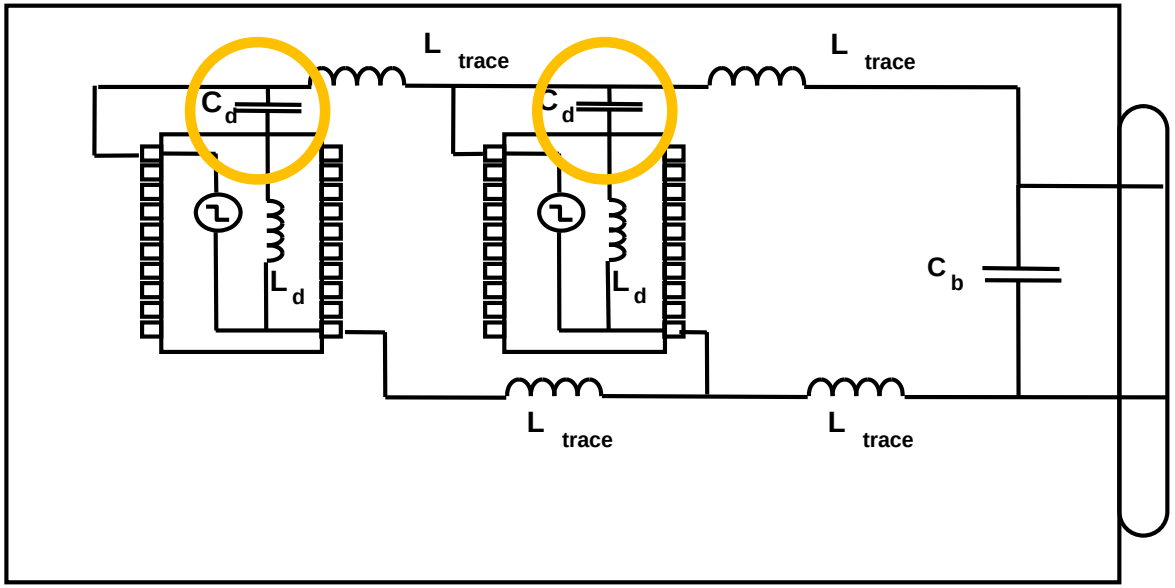


Decoupling Basics
The Concept of Power Bus Decoupling





Decoupling Basics
The Concept of Power Bus Decoupling



PCB Decoupling for 2 Layer PCBs or Single Layer PCBs

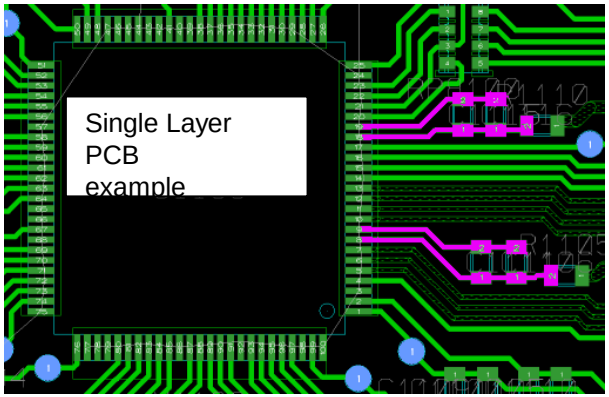
- **Objective:**

  On PCBs with no power planes: To provide adequate charge to the clocked IC at a rate required to reducing integrated circuit power supply emissions from simultaneous switching noise (SSN).

  – Make connections with short trace lengths and avoid vias

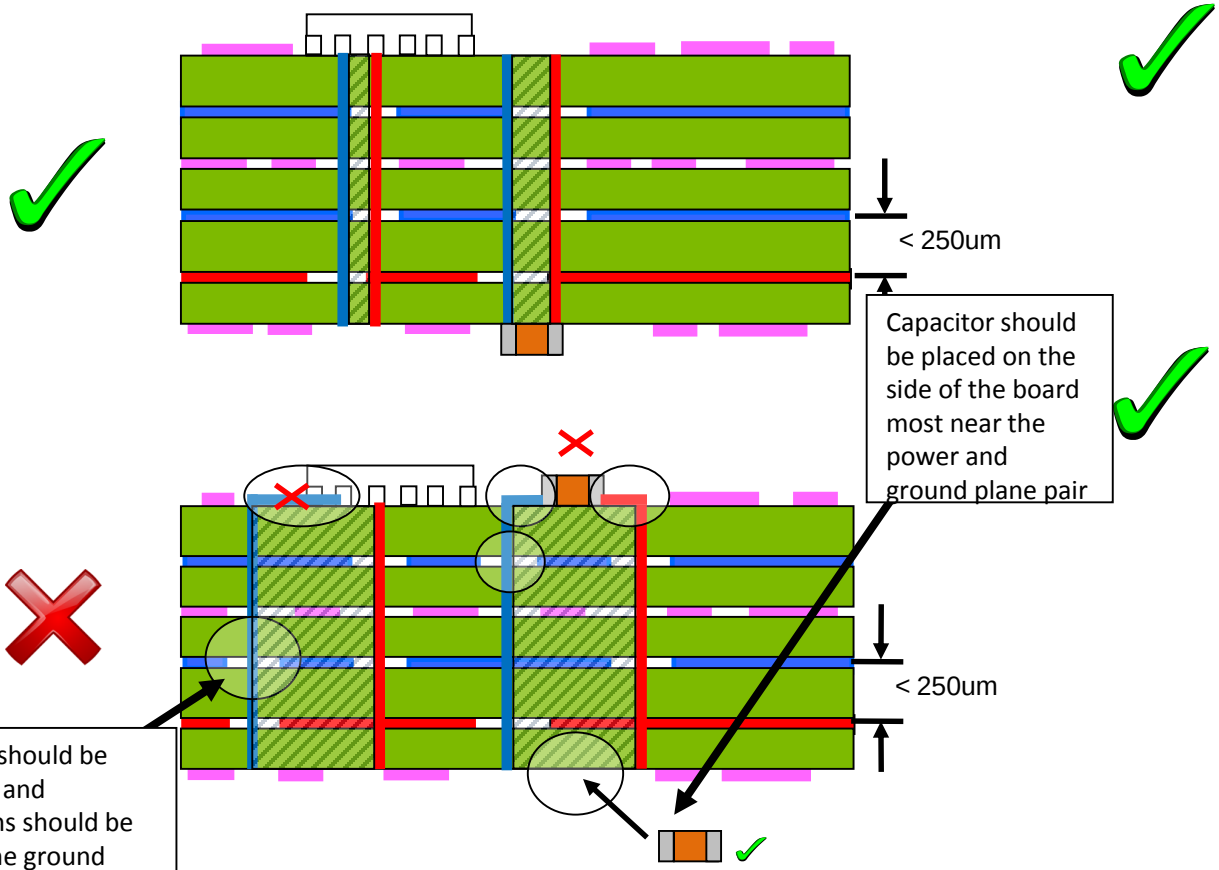
  – Place bulk capacitor close to supply

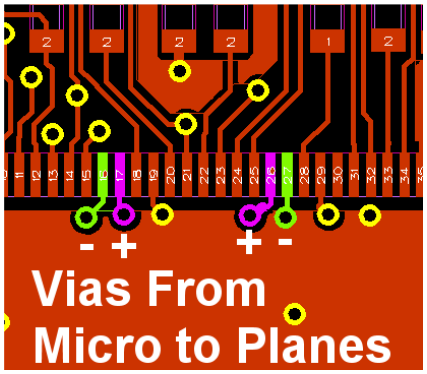
  – In general 2 decoupling capacitors of the same value is better than one capacitor with the same total value of capacitance

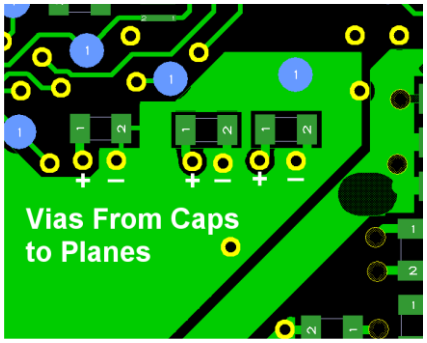


PCB Decoupling for multilayer PCBs < 250um Thickness

= Other
= Power
= Ground





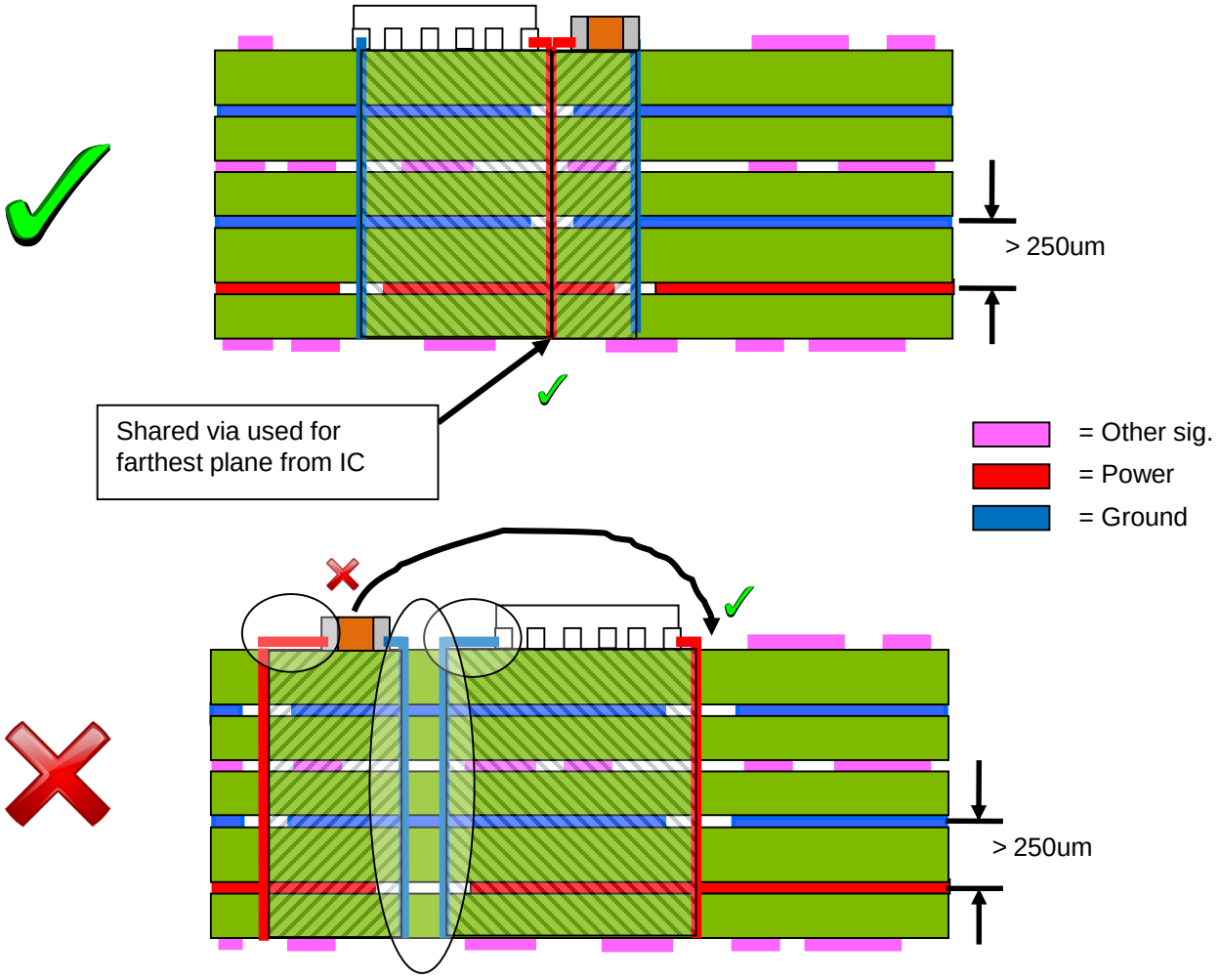


PCB Decoupling for multilayer PCBs < 250um Thickness

- **Objective:** On PCBs with power or ground planes located adjacent to one another in the PCB stack-up and separated less than 250um: To provide adequate charge to the clocked IC at a rate required to reducing integrated circuit power supply emissions from simultaneous switching noise (SSN). Good capacitor decoupling is one part of a power distribution network (PDN).

-
  - In the first few nano-seconds of IC switching most of the current is drawn from the power and ground plane capacitance. Therefore connect microcontroller PWR and GND pins to the planes directly with two vias (one for each pin) located close to each other
  - Location of physical decoupling capacitors is NOT critical. Locate capacitors in general area of IC (flexibility!!)
  - Decoupling capacitors recharge the plane capacitance. Therefore connect capacitors directly to the planes with two vias (one for each pin) located close to each other
  - Mount all capacitors on the side of the board that is closest to the power and ground plane pair in the stack-up

PCB Decoupling for multilayer PCBs > 250um Thickness

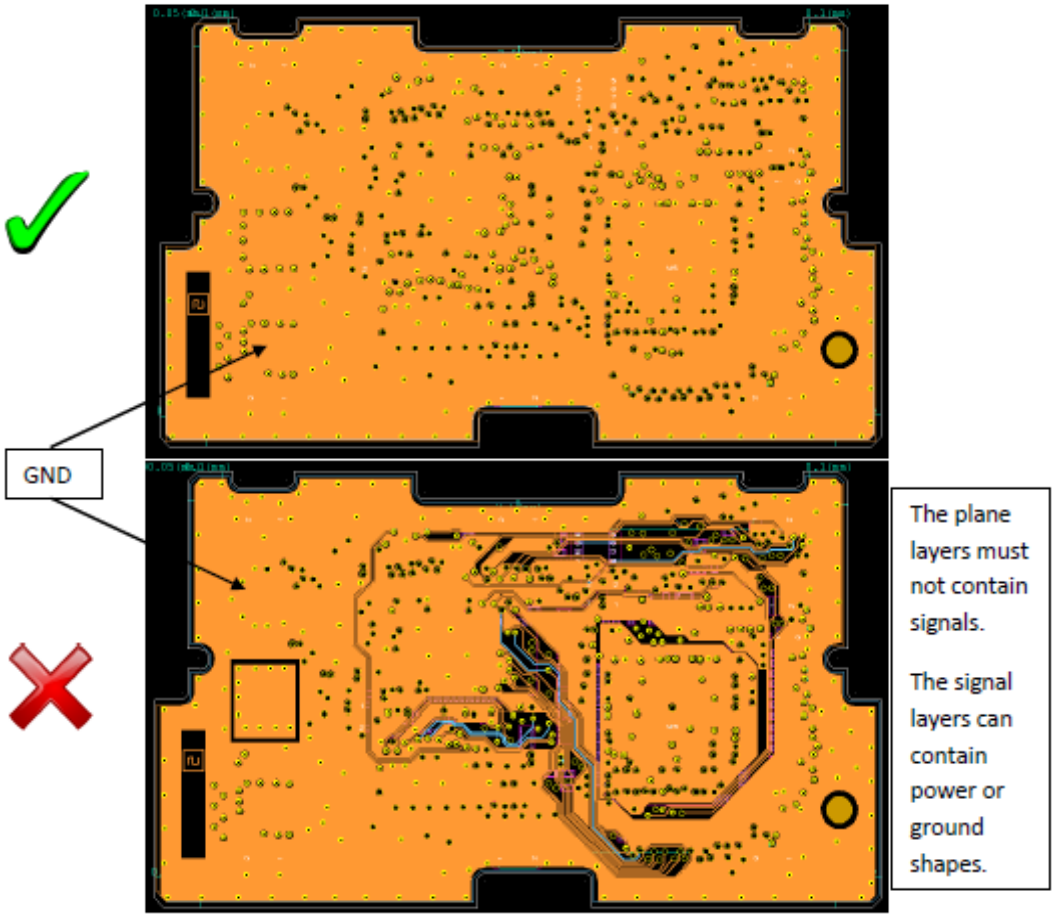


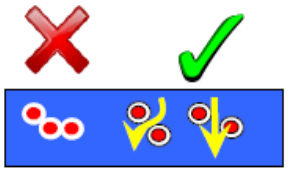
PCB Decoupling for multilayer PCBs > 250um Thickness

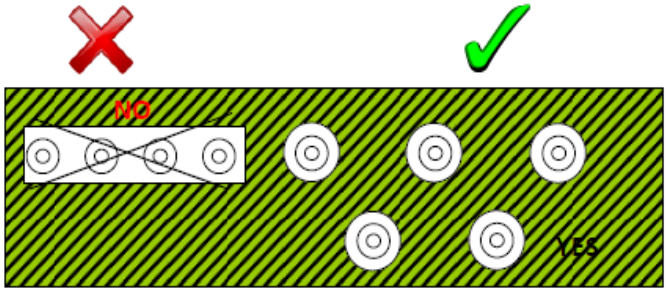
- **Objective:** On PCBs with power or ground planes located adjacent to one another in the PCB stackup and separated by more than 250um: To provide adequate charge to the clocked IC at a rate required to reducing integrated circuit power supply emissions from simultaneous switching noise (SSN). Good capacitor decoupling is one part of a power distribution network (PDN).

-
  - Location of decoupling capacitor is critical. Locate the capacitor near the pin of the active device that will connect to the most distant plane
  - It's optimal if vias can be shared (between cap and IC connection to plane)
  - Connection inductance between IC and decoupling capacitor is critical. Orient the decoupling capacitor so that the pad connected to the most distant plane is near the corresponding active device pin
  - Avoid long trace connections. Inductance is lower by using vias directly
  - For non-BGA ICs, mount all capacitors on the same side of the board as the IC

Use Full Ground Planes in Multi-Layer Printed Circuit Boards (PCBs)

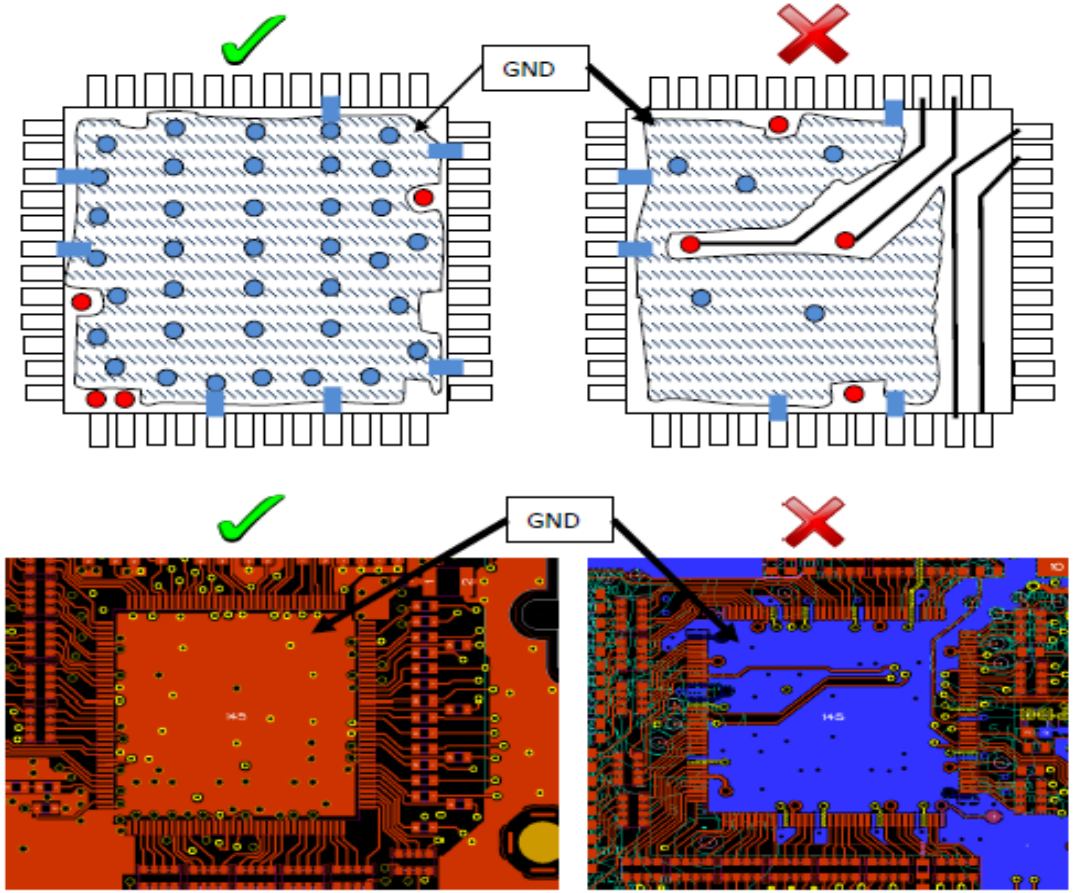






Do Not Allow Breaks in the Copper Areas

Maintain Maximum Ground Fill Under the Integrated Circuits That Use Clock Signal



Location of Terminating Components

Place the series terminating components closest to the driver integrated circuit (IC) and not at the receiver IC

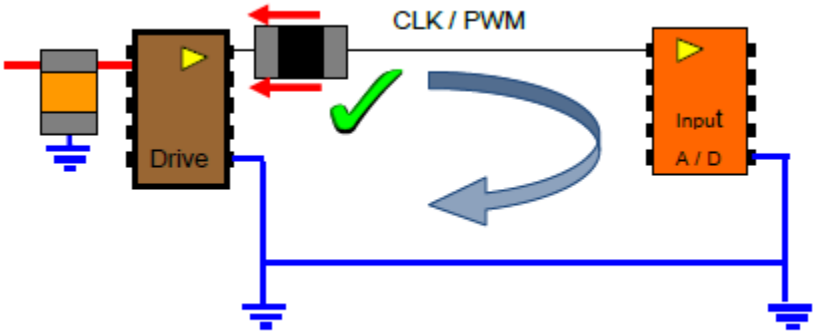
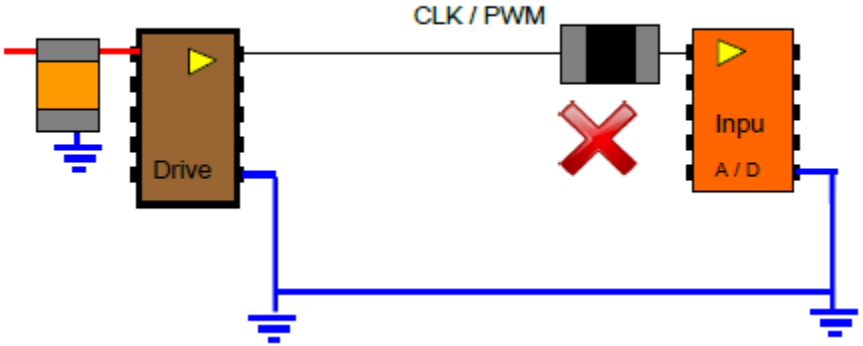
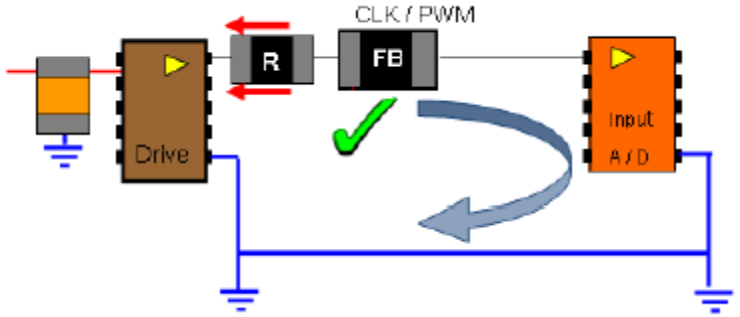


Figure 2: Correct location of the series terminating components.



Placement of Ferrite Beads

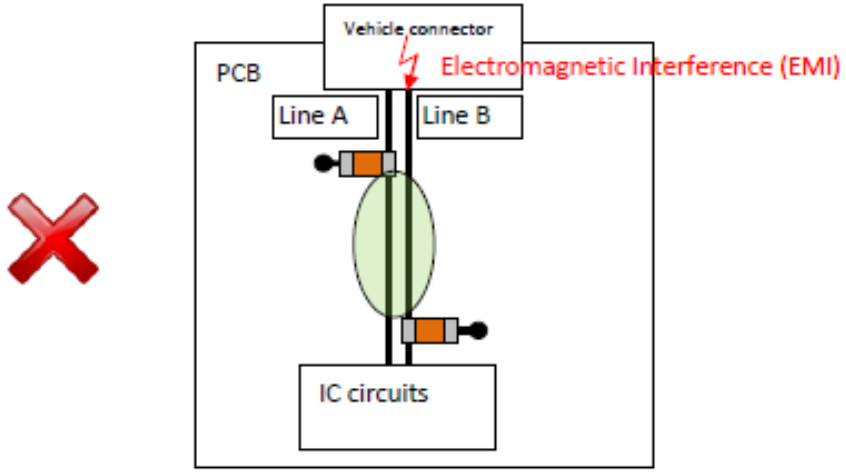
Ferrite beads must be placed as close as possible to the noise source to decrease the noise levels which can cause disturbance of near circuits.

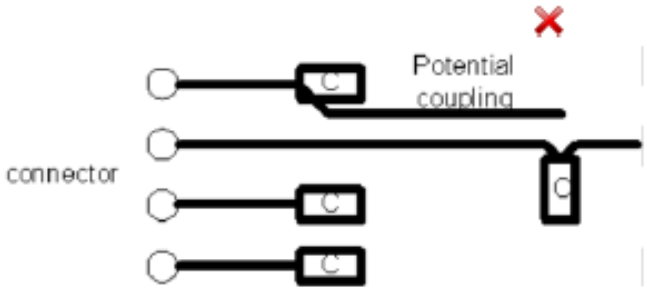


Coupling between signals

Do Not Allow the Coupling Between Parallel Traces of Filtered and Unfiltered Signals.

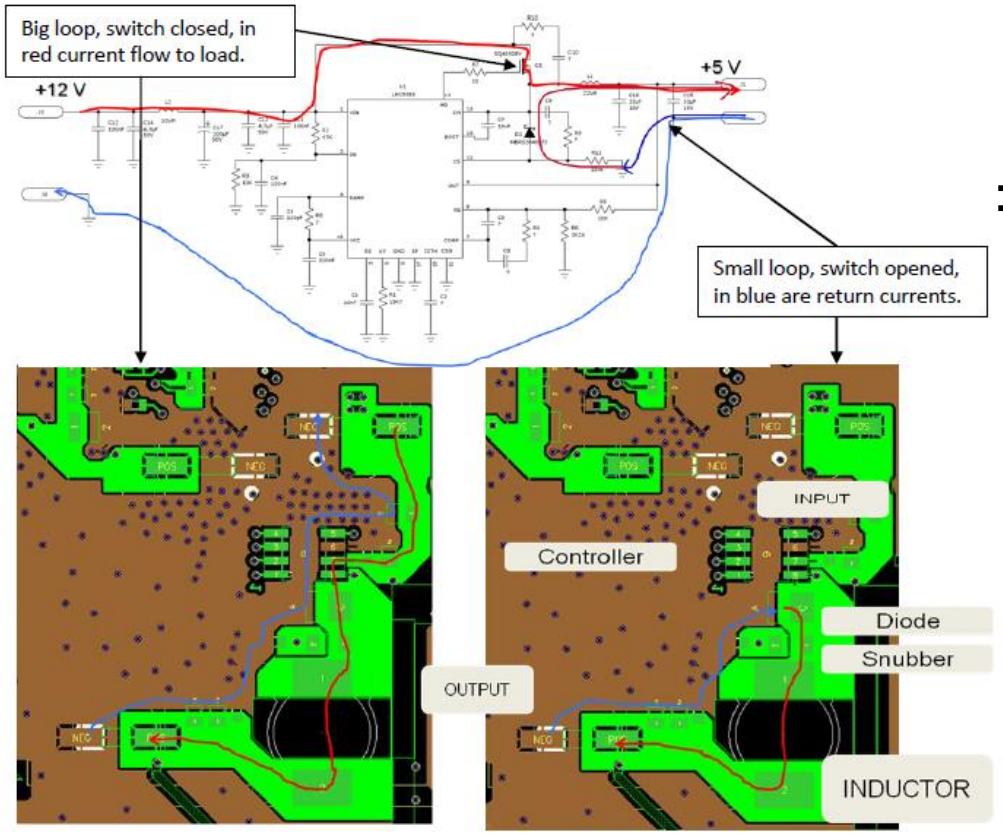
- Make sure that the filter elements are placed near to the connector.
- Do not route in parallel traces with connected filter circuit and without connected filter circuit.





Switch Mode Power Supply

Layout and Placement of Buck Converter



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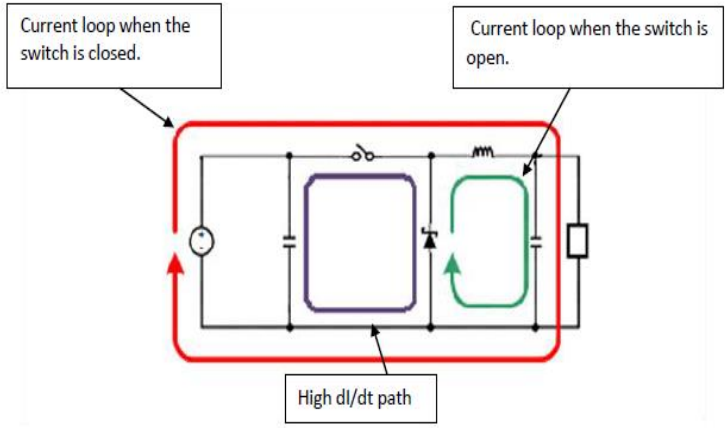
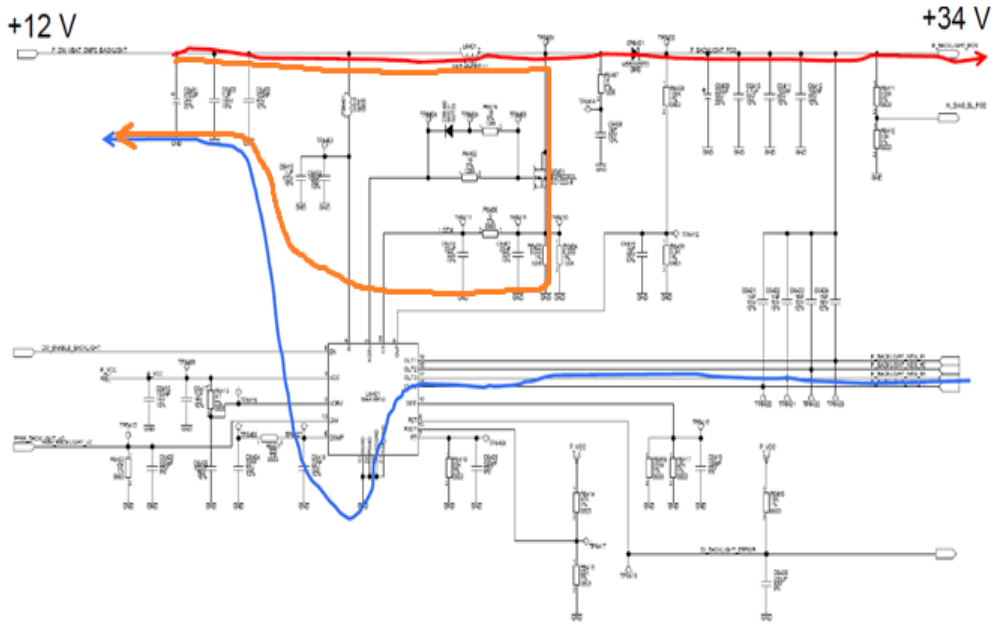


- Keep surface area between FET drain, diode and the inductor as small as acceptable from the thermal point of view.
- Keep the input and output loop areas as small as possible.
- Maintain continuous ground connections from the input through the regulator or FET to the output.
- Keep the diode, snubber, FET, controller, regulator and decoupling capacitors on same side of PCB. Do not use vias.

Switch Mode Power Supply

Layout and Placement of Boost Converter



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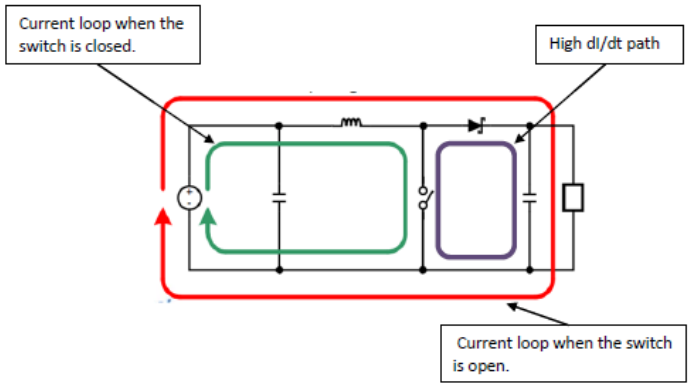

Make the high dI/dt path as short as possible.

- Place the electronic components included in this path as close as possible.
- Connect the source of the low-side FET to the negative pin of the output capacitor first and then make the connection to the ground plane.
- Create the large continuous ground fill below the SMPS