У П Р А Ж Н Е Н И Е № 8

Електронен електромер

В това упражнение студентите се запознават със специализираната интегрална схема **ADE7755** проектирана за работа в устройства за измерване на електрическа мощност и енергия (електронни електромери). Тя може освен за променлив да се използва и за постоянен ток – например за консумираната енергия от акумулатор.

ADE7755 е част от фамилията интегрални схеми на фирмата Analog Devices в която са включени схеми за еднофазни и трифазни измервания, с различен вид изходи, за измерване на активна и реактивна енергия, с различна точност и др.

http://www.analog.com/en/analog-to-digital-converters/energy-measurement/products/index.html.

За самото упражнение студентите трябва предварително да се запознаят със схемата **ADE7755**, схемата на макета и схемите на свързване.

В това упражнение се настройва и проверява работата на макета при **ПРОМЕНЛИВ** ток.

Задачи:

1. Да се разучат материалите **ADE7755**, **AN559** и **AD7751_5eb_0**;

2. Да се подготви план за настройка и проверка на макета. За точка **6** се подготвят таблици при различни стойности на тока, напрежението и фазовата разлика;

3. С помощта на ръководителя на упражнението да се разучи симулаторът на електрическата мрежа ТУ202 (товарно устройство);

4. Да се включи захранването на макета. Да се измерят напреженията в контролните точки. С това се установява началната работоспособност на макета.

5. Да се свържат токовата и напрежителната вериги при **ИЗКЛЮЧЕНО** товарно устройство **ТУ202**. Да се следят изходните сигнали на макета. Не трябва да има съществени изменения.

6. Да се настрои макетът и снеме точността на преобразуване при различни режими на работа.

Точки 1 и 2 се подготвят предварително – домашна работа!

В Н И М А Н И Е !!!

Максималното напрежение което е допустимо да се подава на измервателните входове U и I трябва да се спазва. То е много различно за ток и напрежение и при евентуална размяна макетът ще се повреди!!!

Указания:

Схемата **ADE7755** работи както с променлив, така и с постоянен ток. Тя има логически вход с който може да се зададе работа само с променлив ток. В това упражнение се настройва и проверява работата на макета при ПРОМЕНЛИВ ток и превключвателят трябва да е в съответното положение.

При настройката и проверката се използва специализиран източник на трифазно напрежение и ток **ТУ202 (товарно устройство)**. С този източник се задават токът и напрежението. Неговата точност е достатъчна за извършване на настройките.

Входовете за ток и за напрежение на макета са диференциални – **U***,**U** и **I***,**I**. И на двата входа се подава напрежение.

Безопасните напрежения за измервателните входове **V1** и **V2** на интегралната схема са ±1V. Работните напрежения за които се гарантира точността на преобразуване са по-малки и са съответно 660mV/DC за напрежителния и 470mV/DC за токовия вход.

На входа за напрежение на макета (означен с **U)** максималното работно напрежение е 150V/AC. То е увеличено (от 660mV/DC на 150V/AC) с делител 150к/1к, като делителят може да се настройва с тример-потенциометър .

Максималните работни напрежения са дадени като **амплитудни** стойности – DC. Това означава, че допустимите **ефективни** стойности (при AC сигнал) са по-малки (връзка ефективна – амплитудна стойност).

На входа за ток напрежението може да се подава от шунтов резистор, от токов трансформатор или с помощта на външен съпротивителен делител. Това се задава от положението на мостчетата. Във всички случаи избраната схема на свързване трябва да гарантира безопасни стойности на напрежението на токовия вход < 0,5V.

Когато се ползва токов трансформатор към вторичната намотка непременно трябва да е включен шунтов резистор. В противен случай ще се надвиши максималното допустимото напрежение на токовия вход.

На платката на макета има монтирани два резистора по 51Ω. Те могат да се ползват, ако стойностите им са подходящи за избраната схема на свързване.

Интегралната схема представлява преобразувател на активна мощност в честота. На изходите **F1, F2** и **CF** на схемата се получават импулси с честота която се определя от напреженията на двата входа **V1** и **V2**, фазата между тях, опорното напрежение **REF** и логическите входове **SCF, S0, S1**, както и чувствителността (**G0**, **G1**) на токовия вход.

При изчисляване на връзката между входната мощност и изходната честота трябва да се отчита и делителят на входа на напрежение (на макета) и стойността на външния шунтов резистор.

При подготовката за настройка на макета трябва да се избере коефициентът на съпротивителните делители към входа за напрежение **(V2P**,**V2N)** на интегралната

схема. Този коефициент може да се променя с тример-потенциометъра приблизително два пъти – от 150/1 до 150,5/0,5.

Коефициентите на преобразуване които се определят от логическите входове на схемата (**G0, G1, SCF, S0, S1**) са описани в **ADE7755.pdf**.

Формулата за връзката между напреженията **V1** и **V2**, опорното напрежение **REF** и положението на логическите входове е дадена в **ADE7755.pdf**.

Честотата на импулсите на изходите **F1**, **F2** показва мощността на входа, а броят им съответства на енергията. Мощността се изчислява като измерената честота се умножи по коефициентите на преобразуване. Отчитането на енергията става с броене на импулсите. За по-точно измерване на честотата се използва по-високочестотният изход **CF**. В описанието на **ADE7755** е дадено отношението на честотата **CF** към **F1,F2** в зависимост от положението на логическите входове.

Ред на работа:

При задаване на напрежението и тока на товарното устройство изходите трябва да са в положение СТОП, т.е. светодиодът да не свети. В противен случай при превключването може да се премине през опасни стойности. След като се зададат желаните стойности се натиска бутон СТАРТ, светодиодът свети и на изходите се появяват зададените напрежение и ток.

За да се установи изправността на макета, първо, след включване на захранването се измерват захранващите напрежения **AVdd**, **DVdd** и двете 5V и опорното напрежение **REF** – 2,5V. Сравняват се с допустимите отклонения според каталога.

Измерва се стойността на шунтовия резистор като от товарното устройство се зададе ток и се измери напрежението (изчислява се по закона на Ом).

Настройката на макета, преди измерване на предавателните характеристики, се свежда до настройка на делителите на входа за напрежение (тримери 500Ω).

Проверката на макета се прави при различни стойности на напрежение, ток и фазова разлика. Проверява се линейността на преобразуване. Определя са зависимостта между входната мощността на входа и честотата в изхода. За по-точно измерване се използва високочестотния изход **CF**.

1. Настройка на делителите на входа U за напрежение

Входният обхват може да бъде между 50 и 120V (определен е от стойностите на резисторите). Той се избира в зависимост от изходната честота която ще се получи на **F1**, **F2** – отчитането да е число кратно на 10, т.е 1Hz да съответства на 0,1W, на 1W, на 10W, 100W и т.н. Избраният обхват, респективно коефициент на делене участва във формулата задаваща връзката входна мощност – изходна честота.

На входа на макета **U*** се подава напрежение съответстващо на избрания обхват. То се отчита на индикатора на товарното устройство. С потенциометрите се настройва избраният коефициент на делене (напрежението след делителя се измерва директно на съответния вход на интегралната схема – 7 или 8 спрямо нулата).

Трябва да се внимава да не се надвишава максималната допустима стойност на входа за напрежение – 660mV DC. **Подаваното напрежение е променливо**.

За да се настроят еднакво двата делителя (към **V2P**,**V2N**) едновременно се подава едно и също напрежение към двата входа или се разменят двата свързващи проводника.

За да се провери дали настройката на двата входа **U***,**U** е извършена правилно, на двата свързващи проводника се подава едно и също напрежение и се измерва напрежението между двата входа на интегралната схема при максимална чувствителност на волтметъра.

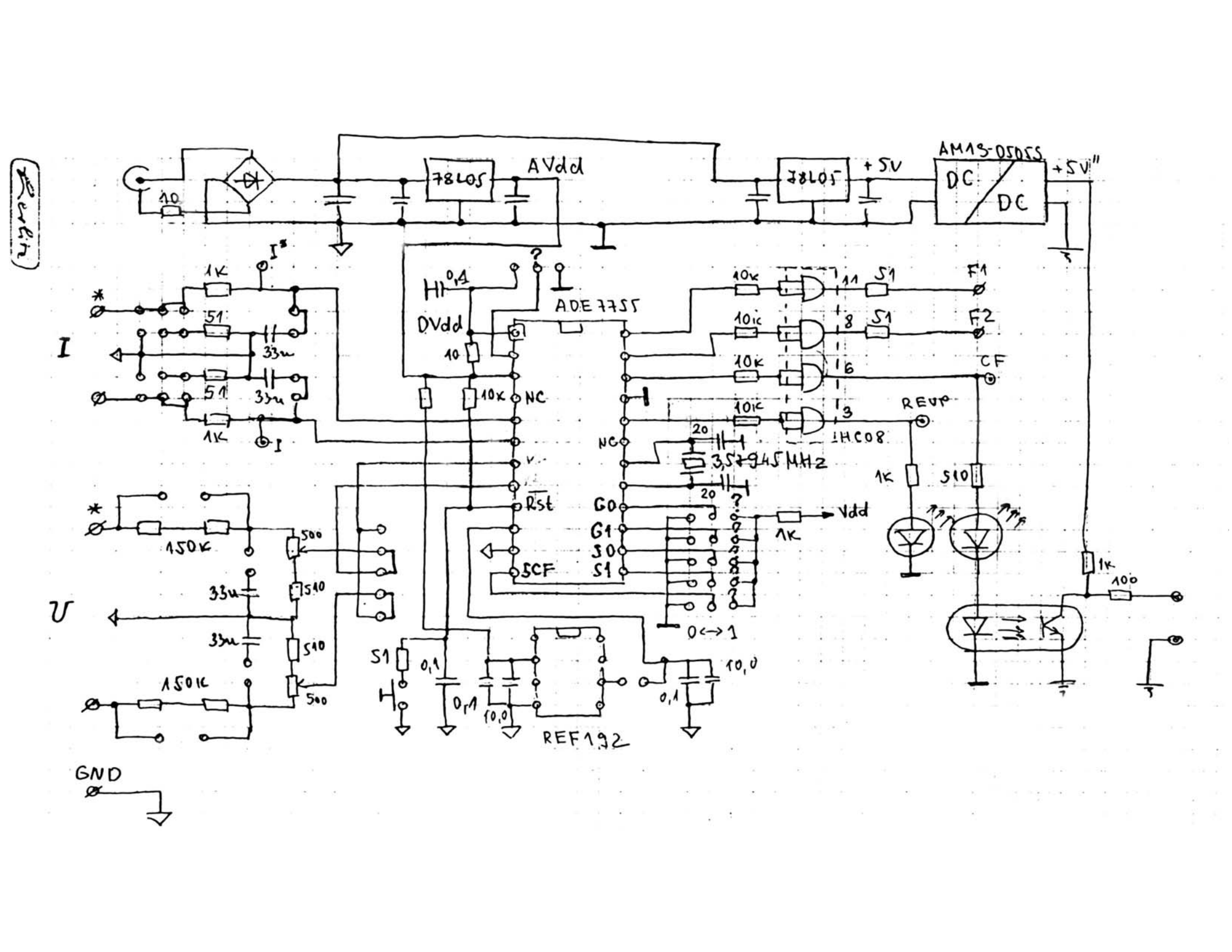
Същата проверка може да се направи и като се измерва изходната честота на изход CF на макета. Задава се ток 1-2A, напрежение близко до избраното за обхват. Отчита се честотата като се разменят местата на двата проводника за напрежение. Честотата не трябва да се променя, а диодът REVP трябва да сменя състоянието си.

2. Проверка на работата на електромера

За целта, в предварително подготвени таблици се нанасят стойностите на изходната честота за различни напрежения, токове и фазова разлика.

Проверява се работният обхват при различните коефициенти на усилване на токовия канал.

Сравняват се получените данни с изчислените по формулата за преобразуване.


Zentrale
10
7805
AVdd
7805
+5V
AM1S-0505S
DC
DC
+5V"
I
U
1K
51
33u
51
33u
1K
I
*
150K
500
510
33u
33u
510
150K
500
S1
0,1
0,1
10,0
10,0
0,1
REF192
GND
HI
0,1
DVdd
10
ADE7755
10K
NC
Rst
SCF
NC
G0
G1
S0
S1
0<->1
1K
Vdd
10K
11
S1
F1
10K
8
S1
F2
10K
6
CF
10K
3
REVP
74HC08
20
3,5795MHz
20
1K
510
1K
100

Evaluation Board Documentation
AD7751/AD7755 Energy Metering IC

EVAL-AD7751/AD7755EB

FEATURES

Single +5 V Power Supply
Easy Connection of External Transducers via Screw Terminals
Easy Modification of Signal Conditioning Components Using PCB Sockets
Trim Pot for Analog Calibration of Meter Constant
LED Indicators on Logic Outputs for Fault (AD7751 Only), REVP and CF
Optically Isolated Output for Calibration/Test Purposes
External Reference Option Available for Reference Evaluation

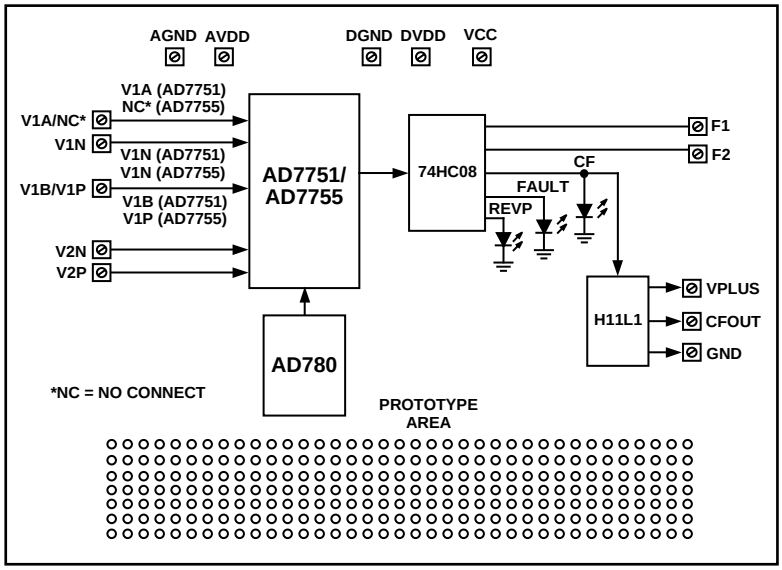
GENERAL DESCRIPTION

The AD7751 and AD7755 are high accuracy energy measurement ICs. The part specifications surpass the accuracy requirements as quoted in the IEC1036 standard. The AD7751 incorporates a novel fault detection scheme that both warns of fault conditions with the logic output FAULT but allows the AD7751 to continue accurate billing during a fault event. The AD7751 does this by continuously monitoring both the phase and neutral (return) currents. A fault is indicated when these currents differ by more than 12.5%. Billing is continued using the larger of the two currents. The FAULT output is connected to an LED on the evaluation board.

The AD7751 supplies average real power information on the low frequency outputs F1 and F2. These logic outputs may be used to directly drive an electromechanical counter or interface to an MCU. The evaluation board provides screw connectors for easy connection to an external counter. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes. The evaluation board allows this logic output to be connected to an LED or optoisolator. The REVP logic output goes high when negative real power is detected. This causes an LED on the evaluation board to switch on.

The AD7751/AD7755 evaluation board can easily be converted into an energy meter by the addition of a local power supply and the connection of the appropriate transducers. A large amount of prototype area is made available on the evaluation board for this purpose.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

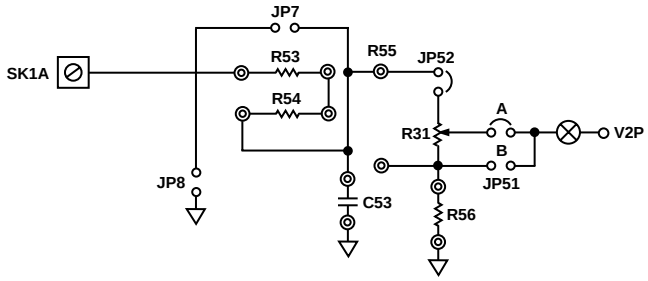
One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ANALOG INPUTS (SK1 AND SK2)

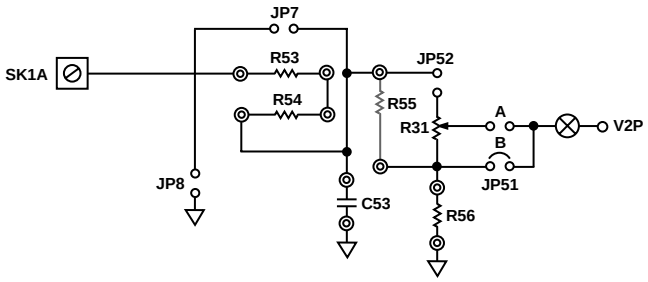
Voltage and current signals are connected at the screw terminals SK1 and SK2 respectively. All analog input signals are filtered using the on-board antialias filters before being presented to the analog inputs of the AD7751 or AD7755. Some analog inputs offer additional signal conditioning, e.g., attenuation on the voltage channel. The default component values shipped with the evaluation board are the recommended values to be used with the AD7751 and AD7755. The user can easily change these components, however this is not recommended unless the user is familiar with sigma-delta converters and also the criteria used for selecting the analog input filters—see AD7751 and AD7755 data sheets.

Voltage Input

SK1 is a two-way connection block that can be directly connected to a high voltage source, e.g., 220 V rms. The resistor network R53, R54, R55, R56 and R31 make up a very flexible attenuation and calibration network—see schematic. The attenuation network is designed such that the corner frequency (–3 dB frequency) of the network matches that of the RC (antialiasing) filters on the other analog inputs. This is important, because if they do not match there will be large errors at low power factors. Figure 1 shows how the attenuation network may be used with fixed resistors or the trim pot. The trim pot allows the voltage signal on V2P to be scaled to calibrate the frequency on CF to some given constant, e.g., 3200 imp/kWhr. Some examples are given later.



a. Attenuation Using Trim Pot (R31)



b. Attenuation Using Fixed Resistors

Figure 1. Attenuation Network on Channel 2

If Channel 2 is being used in a single-ended mode of operation, the unused input of the pair should be connected to analog ground (AGND) via an antialias filter. This is shown in Figure 2 where V2N is connected to AGND using jumper JP10.

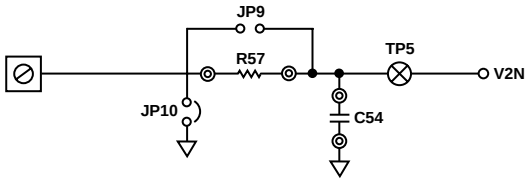


Figure 2. Unused Analog Inputs Connected to AGND

All passive components (resistors and capacitors) which make up the attenuation network and antialias filters may be modified by the user. The components at mounted using PCB jack sockets which allow for easy removal and replacement of components.

Current Input

SK2 is a three-way connection block which allows the AD7751/AD7755 to be connected to a current transducer. The AD7751 has three inputs which are used with two current transducers, e.g., two CTs (current transformers). The AD7755 has one differential input channel for connection to the current transducer, i.e., two inputs. When using the AD7755 in the evaluation board the input SK2A is not used. PCB jack sockets allow CT burden resistors to be placed on the evaluation board at positions SH1 and SH2. Figures 3 and 4 show some typical connection diagrams for CT and shunt connection.

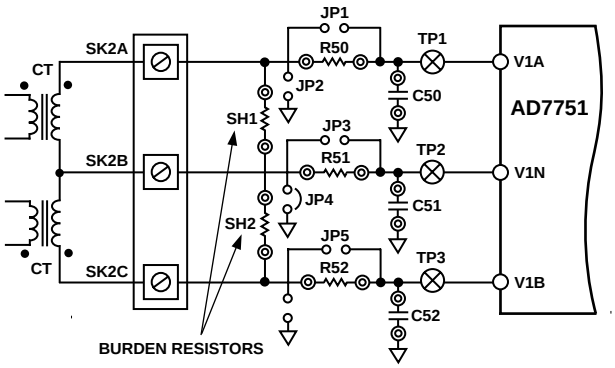


Figure 3. Typical Connection for Channel 1 of the AD7751

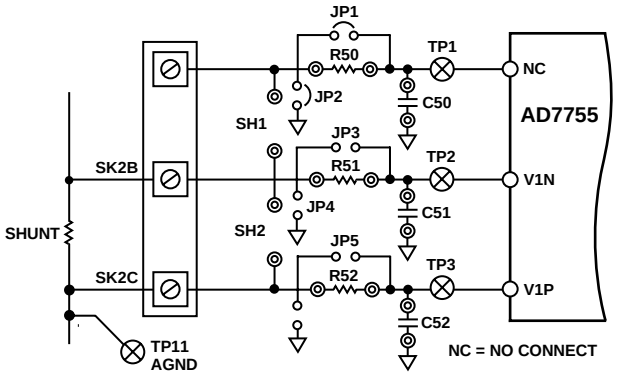


Figure 4. Typical Connection for Channel 1 of the AD7755

AD7751/AD7755 EVALUATION BOARD SETUP

Figure 5 shows how the AD7751/AD7755 evaluation board can be set up for a simple evaluation. Two signal generators are used to provide the sinusoidal (ac) signals for Channel 1 and Channel 2. The user must have some way of phase locking the generators. This will ensure that the sinusoidal signals remain in phase. Also if the AD7751 and AD7755 performance-over-power factor is being evaluated, two separate signal sources will be required. The generators are shown connected in a single-ended configuration. The grounded analog inputs of Channel 1 and Channel 2 (V1N and V2N) are connected to AGND via an antialias filter. In Figure 5, analog input V2N is grounded via R55 and R56. The capacitor C53 is connected in parallel.

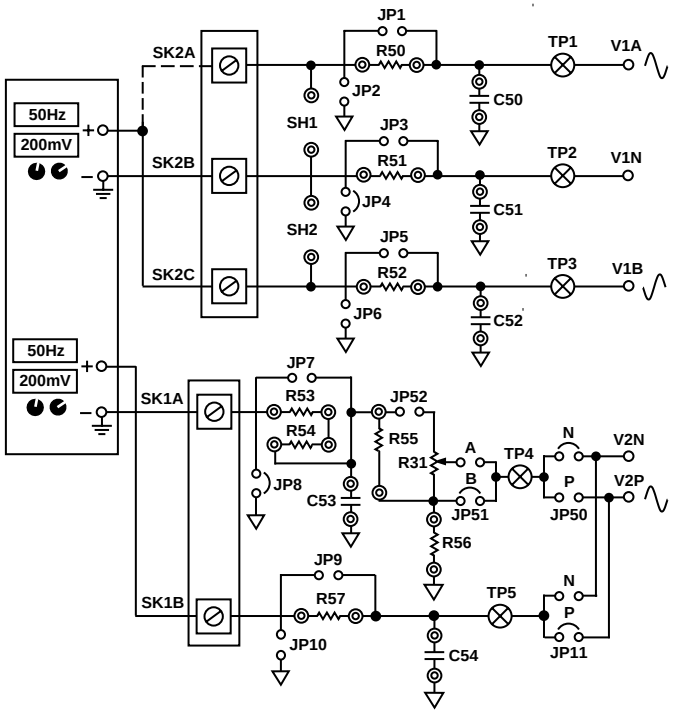


Figure 5. Typical Connection for Analog Inputs

LOGIC OUTPUTS

AD7751 and AD7755 provide the active power information in the form of an output frequency. The three frequency outputs are F1, F2 and CF. Consult the AD7751 and AD7755 data sheets for more information on these outputs. The logic outputs F1 and F2 are intended to be used to drive an impulse counter or stepper motor. The outputs are buffered and available at the connector SK6. A stepper motor may be directly connected here. The power supply for the buffer is VCC (SK4A) and may be connected to either the AD7751/AD7755 supply using jumper JP21, or to its own supply.

The logic output CF can be directly connected to an LED using JP19 (Position B) or to an optically isolated output (Position A). By closing Positions A and B, both options are selected. The optically isolated output is available at connector SK5. This isolated output is useful when the evaluation board is connected directly to a high voltage (e.g., 220 V residential). A typical connection diagram for this isolated output is shown in Figure 6.

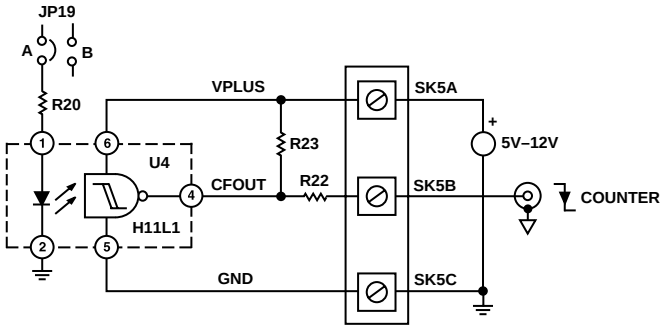


Figure 6. Typical Connection for Opto Output

The logic output REVP indicates negative power measurement. Since the frequency outputs can only convey magnitude information, the sign of the power calculation is given by the REVP logic output. For more information regarding this output see the AD7751/AD7755 data sheet. This output is connected to an LED on the evaluation board. The LED will be illuminated if negative power is detected.

The AD7751 also has a logic output called FAULT. This output goes active when the signal levels on V1A and V1B differ by more than 12.5% (see Figure 3). This output is also connected to an LED on the evaluation board. Jumper J22 should be open when evaluating the AD7751.

All logic outputs can be monitored via test points 6 to 10 (TP6 to TP10). These test points provide easy access for scope probes and meter probes.

AD7751/AD7755 OUTPUT FREQUENCY SELECTION

AD7751 and AD7755 provide up to four different output frequencies on F1 and F2. The output frequency selection is made via the logic inputs S0 and S1—see AD7751/AD7755 data sheet. On the evaluation board these inputs are set by using jumpers JP15 and JP16. The logic input SCF is set via jumper 14 (JP14). For a full explanation of the AD7751/AD7755 output frequency selection see the data sheet.

AD7751/AD7755 INPUT GAIN SELECTION

AD7751 and AD7755 provide up to four different gain settings on the analog input Channel 1. These gain settings are 1, 2, 8 and 16. The gain selection on the evaluation board is made via JP17 and JP18.

EXTERNAL CLOCK INPUT

AD7751 and AD7755 are specified with a CLKIN value of 3.579545 MHz. The evaluation board uses a crystal of this value for the on-chip gate oscillator circuit. However, an input is provided to allow an external clock source to be used. An impedance matching resistor (R11) of 50 Ω is also available on the board. NOTE: when using the on-chip oscillator this resistor must be removed or the on-chip oscillator circuit will not start up.

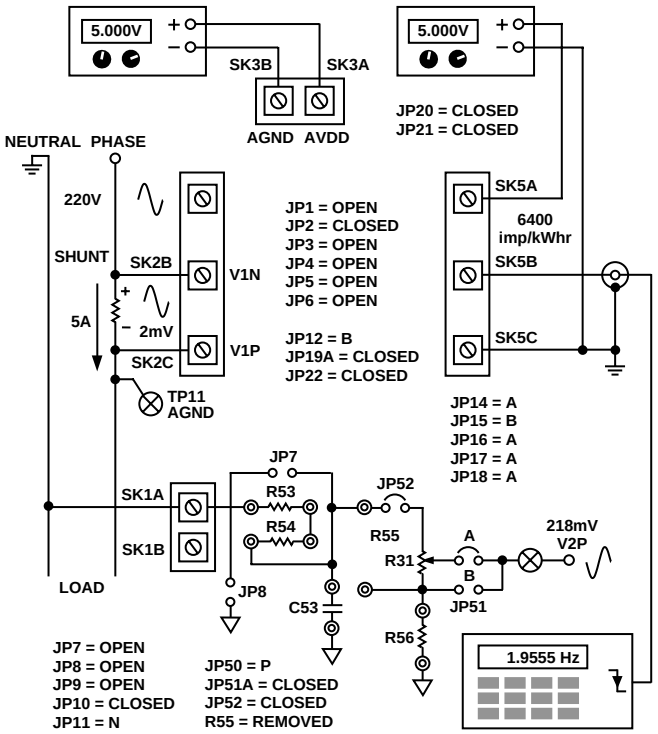


Figure 7. AD7755 Evaluation Board as an Energy Meter

AD7755 EVALUATION BOARD SET UP AS AN ENERGY METER

Figure 7 shows a wiring diagram that allows a simple energy meter to be implemented using the AD7755 evaluation board. The current transducer used in this example is a shunt (400 μΩ). The meter is intended to be used with a line voltage of 220 V and a maximum current of 25 A. The frequency outputs F1 and F2 can be used to drive a mechanical counter. These outputs will be calibrated to provide 100 imp/kWhr. The logic output CF has an output frequency that can be up to 128 times higher than the frequency on F1 and F2. This output can be used for calibration purposes and is shown connected to a frequency counter via the optoisolator in Figure 7.

At maximum current (25 A), the power seen by the meter will be 5.5 kW. This will produce a frequency of 0.153 Hz on F1 and F2 when these outputs are calibrated to 100imp/kWhr (100imp/hr = 0.02777 Hz, 0.02777 × 5.5 = 0.153 Hz). From Table III in the AD7755 data sheet, the closest frequency to 0.153 Hz in the half-scale ac inputs column is for F_2, i.e., 0.17 Hz. Therefore F_2 is selected by setting S0 = 1 and S1 = 0. The choice of CF frequencies in this mode (see Table IV in the AD7755 data sheet) are 32 times F1 and 64 times F1. For this example 64 times F1 is selected by setting SCF = 1.

Since the voltage on Channel 1 is fixed, the only possible way of calibrating (adjusting) the output frequency in F1 and F2 is by varying the voltage on Channel 2. This is carried out by varying the attenuation of the line voltage using the trim pot.

First we can calculate the voltage required in Channel 2 in order to calibrate the frequency on the logic outputs F1 and F2 to 100imp/kWhr. The AD7755 data sheet gives the equation which relates the voltage on Channel 1 and Channel 2 to the output frequency on F1 and F2.

$$Freq = \frac{8.06 \times V1 \times V2 \times Gain \times F_{1-4}}{V_{REF}^{\ 2}} \quad (1)$$

First a current is selected for calibration, 5 A for example. This gives a Channel 1 voltage of 400 μΩ × 5 A = 2 mV rms. The gain of Channel 1 on the AD7755 is set to 16 (G0 = G1 = 1). The on-chip or external reference of 2.5 V is selected using JP13.

The output frequency at 5 A on F1 and F2 should be 0.02777 Hz (100imp/kWhr) × 1.1 (220 V × 5 A = 1.1 kW) = 0.03055 Hz.

From Equation 1 the voltage on Channel 2 should be set to 218 mV. The attenuation network as shown in Figure 1 is used to attenuate 220 V to 218 mV. R53 = 660 kΩ, R54 = 100 kΩ, R56 = 500 Ω and the trim pot R31 = 500 Ω.

However, since the meter is being calibrated at CF and CF is set to 64 times F1, the voltage on Channel 2 should be adjusted until CF = 64 × 0.03055 Hz = 1.9555 Hz is registered on the frequency counter. The counter should be set up to display the average of ten frequency measurements on CF. This will remove any ripple due to the instantaneous power signal. See the AD7755 data sheet for more details.

AD7751 EVALUATION BOARD SET UP AS AN ENERGY METER

Figure 8 shows a wiring diagram that allows a simple energy meter to be implemented using the AD7751 evaluation board. Because the AD7751 monitors both the phase and neutral currents, isolation is required on at least one of the current transducers. One convenient way to provide isolation and eliminate problems with matching is to use two CTs (current transformers). The CTs are connected as shown in Figure 8. The CTs have a turns ratio of 1:2500. The burden resistance for the CTs can be placed on the evaluation board at SH1 and SH2. The meter is intended to be used with a line voltage of 240 V and a maximum current of 60 A. The frequency outputs F1 and F2 can be used to drive a mechanical counter. These outputs will be calibrated to provide 100 imp/kWhr. The logic output CF has an output frequency that can be up to 128 times higher than the frequency on F1 and F2. This output can be used for calibration purposes and is shown connected to a frequency counter via the optoisolator in Figure 8.

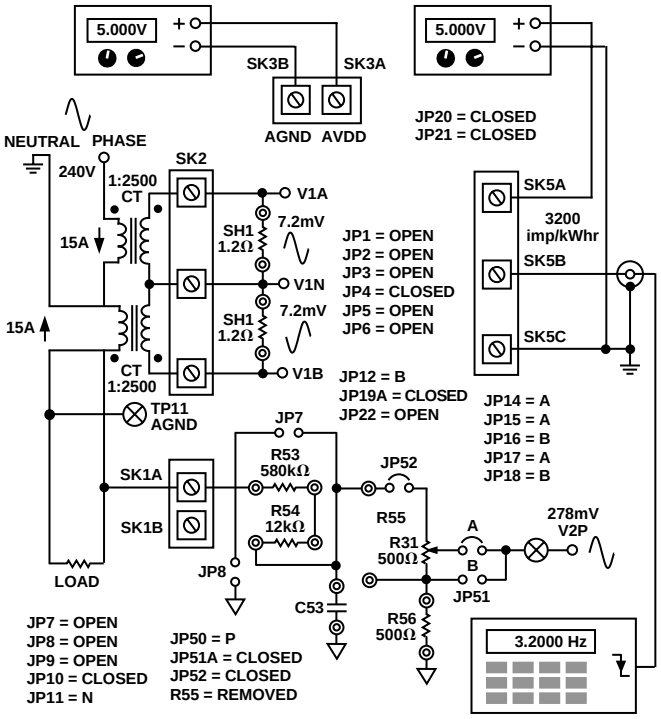


Figure 8. AD7751 Evaluation Board as an Energy Meter

At maximum current (60 A) the power see by the meter will be 14.4 kW. This will produce a frequency of 0.4 Hz on the logic outputs F1 and F2 when these outputs are calibrated to 100imp/kWhr (100imp/hr = 0.02777 Hz, 0.02777 × 14.4 = 0.4 Hz). From Table III in the AD7751 data sheet, the closest frequency to 0.4 Hz in the half-scale ac inputs column is for F_3, i.e., 0.34 Hz. Therefore F_3 is selected by setting S0 = 0 and S1 = 1. The choice of CF frequencies in this mode (see Table IV in the AD7751 data sheet) are 16 times F1 and 32 times F1. For this example 32 times F1 is selected by setting SCF = 1.

Since the voltage on Channel 1 is fixed, the only possible way of calibrating (adjusting) the output frequency on F1 and F2 is by varying the voltage on Channel 2. This is carried out by varying the attenuation of the line voltage using the trim pot.

First we can calculate the voltage required on Channel 2 in order to calibrate the frequency on F1 and F2 to 100imp/kWhr. The AD7751 data sheet gives the equation which relates the voltage on Channel 1 and Channel 2 to the output frequency on F1 and F2.

$$Freq = \frac{5.74 \times V1 \times V2 \times Gain \times F_{1-4}}{V_{REF}^{\ 2}} \quad (2)$$

First a current is selected for calibration, 15 A for example. This gives a Channel 1 voltage of 15 A/2500 × 1.2 Ω = 7.2 mV rms. The gain of Channel 1 on the AD7755 is set to 8 (G0 = 0, G1 = 1). The on-chip or external reference of 2.5 V is selected using JP13.

The output frequency at 15 A on F1 and F2 should be 0.02777 Hz (100imp/kWhr) × 3.6 (240 V × 15 A = 3.6 kW) = 0.1 Hz.

From Equation 2 the voltage on Channel 2 should be set to 278 mV. The attenuation network as shown in Figure 1 is used to attenuate 240 V to 278 mV. R53 = 580 kΩ, R54 = 12 kΩ, R56 = 500 Ω and the trim pot R31 = 500 Ω.

However since the meter is being calibrated at CF and CF is set to 32 times F1, the voltage on Channel 2 should be adjusted until CF = 32 × 0.1 Hz = 3.2 Hz is registered on the frequency counter. The counter should be set up to display the average of ten frequency measurements on CF. This will remove any ripple due to the instantaneous power signal. See the AD7751 data sheet for more details.

JUMPER SELECTION

The AD7751/AD7755 evaluation board comes with several jumper selections that allow the user to exercise all of the AD7751 and AD7755 functionality. There are also some options such as attenuation networks and optically isolated outputs that allow the AD7751 and AD7755 to be evaluated under the same conditions as the end application. Table I outlines all the jumper options and explains how they are used. Table I should be used in conjugation with Figure 9, which will make it easier to locate the jumper in question.

Table I.

Jumper	Option	Description
JP1	Closed	Closing this jumper will short resistor R50 and connect analog input V1A directly to SK2A. This has the effect of removing the antialias filters from this input.
	Open	Antialias filter in input V1A is enabled.
JP2	Closed	Analog input V1A is connected to analog ground (AGND) via the antialias filter.
	Open	Normal operation.
JP3	Closed	Closing this jumper will short resistor R51 and connect analog input V1N directly to SK2B. This has the effect of removing the antialias filters from this input.
	Open	Antialias filter in input V1A is enabled.
JP4	Closed	Analog input V1N is connected to analog ground (AGND) via the antialias filter. This jumper should be closed if the AD7751 is being used as these inputs are used single-ended on the AD7751.
	Open	When evaluating the AD7755, Channel 1 is best used in a differential mode and this jumper should be left open. An example is shown in Figure 4. In this example a shunt is used to sense the current. The shunt can be referenced to the AGND of the board by using TP11 as shown.
JP5	Closed	Closing this jumper will short resistor R52 and connect analog input V1B (V1P AD7755) directly to SK2C. This has the effect of removing the antialias filters from this input.
	Open	Antialias filter in input V1A (V1P) is enabled.
JP6	Closed	Analog input V1B (V1P) is connected to analog ground (AGND) via the antialias filter.
	Open	Normal operation.
JP7	Closed	Closing this jumper will short resistors R53 and R54. The analog input V2P is connected directly to SK1A. This has the effect of removing the antialias filter and attenuation network from this input. Note: if the board is being connected to a high voltage, this jumper must be left open.
	Open	Antialias filter and attenuation network on the input V2P is enabled.
JP8	Closed	Analog input V1A is connected to analog ground (AGND) via the antialias filter. Note: SK1A is also connected to AGND and care should be taken if this input is connected to a high voltage source.
	Open	Normal operation.
JP9	Closed	Closing this jumper will short resistor R57 and connect analog input V2N directly to SK2B. This has the effect of removing the antialias filters from this input.
	Open	Antialias filter in input V2N is enabled.
JP10	Closed	Analog input V2N is connected to analog ground (AGND) via the antialias filter. This option should be selected if Channel 2 is being used in a single-ended mode.
	Open	V2N connected to SK2B for differential operation.
JP11	N	SK1B connected to V2N (AD7751/ AD7755).
	P	SK1B connected to V2P (AD7751/ AD7755).
JP12	A	Logic input AD/$\overline{DC}$ is connected to DGND.
	B	Logic input AD/$\overline{DC}$ is connected to DVDD.
JP13	Open	AD7751/AD7755 internal (on-chip) reference selected.
	Closed	External (AD780) reference selected.
JP14	1	SCF connected to DVDD.
	0	SCF connected to DGND.
JP15	1	S1 connected to DVDD.
	0	S1 connected to DGND.
JP16	1	S0 connected to DVDD.
	0	S0 connected to DGND.
JP17	1	G1 connected to DVDD.
	0	G1 connected to DGND.
JP18	1	G0 connected to DVDD.
	0	G0 connected to DGND.

Jumper	Option	Description
JP19	A	CF logic output connected to optically isolated output at SK5.
	B	CF logic output connected to LED.
JP20	Closed	AVDD and DVDD connected together.
JP21	Closed	DVDD and VCC connected together.
JP22	Closed	Output FAULT (NC on AD7755) is connected to DGND via R7. JP22 should be closed when using the AD7755.
	Open	Should be open when evaluating the AD7751. Leaving closed will disable the FAULT LED.
JP50	N	SK1A connected to V2N (AD7751/ AD7755).
	P	SK1A connected to V2P (AD7751/ AD7755).

Jumper	Option	Description
JP51	A	Trim pot R31 is connected to V2P (depending on the position of JP50)—see Figure 1. This allows the AD7751/ AD7755 output frequency to be scaled using the voltage on V2P.
	B	When option B is selected, the jumper JP52 should be left open. In this configuration the attenuation for V2P is provided via the fixed resistors R53, R54, R55 and R56.
JP52	Open	When open, the attenuation on V2P is provided by fixed resistor as explained above. Also see Figure 1.
	Closed	When closed, the trim pot becomes part of the attenuation network. In this mode of operation the resistor R55 should be removed from its PCB jack sockets.

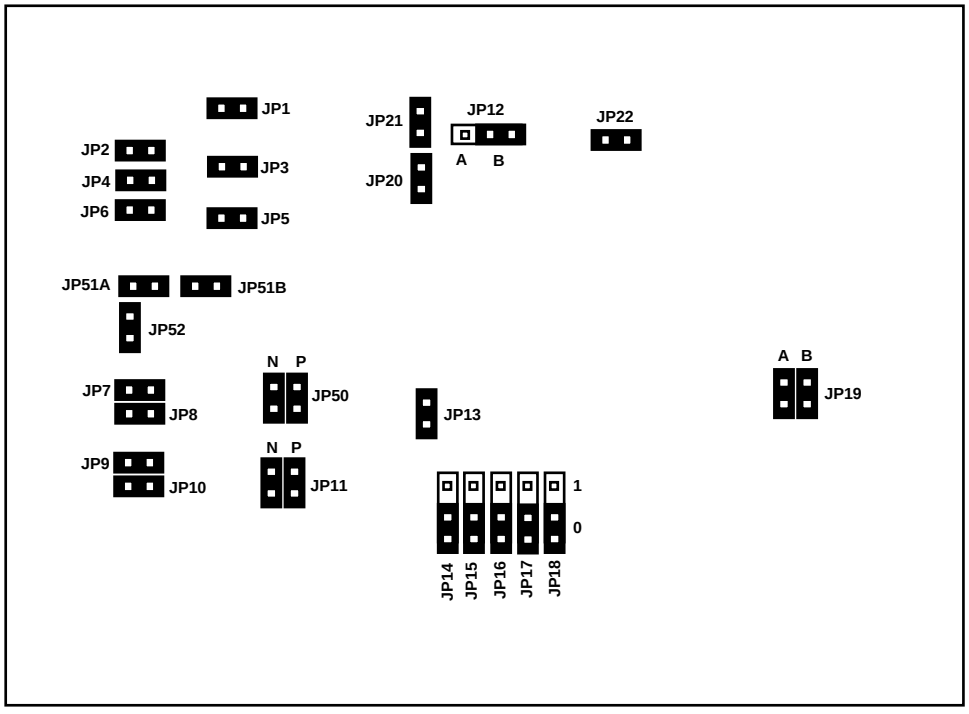


Figure 9. AD7751/AD7755 Evaluation Board Jumper Positions

Evaluation Board Bill of Material

Designator	Value	Description
R1, R2, R3, R4, R5, R23	1 kΩ, 5%, 1/4 W	Resistor, No Special Requirements.
R6, R22	100 Ω, 5%, 1/4 W	Resistor, No Special Requirements.
R7, R8, R9, R10, R58	10 kΩ, 5%, 1/4 W	Resistor, No Special Requirements.
R11	51 Ω, 1%, 1/4 W	FARNELL Part No. 335-629. Not placed unless external clock is being used.
R14, R18, R19, R20	820 Ω, 5%, 1/4 W	Resistor, No Special Requirements.
R16, R17	20 Ω, 5%, 1/4 W	Resistor, No Special Requirements.
R31	500 Ω, 10%, 1/2 W	Trim Pot Resistor, 25 Turn. BOURNS. FARNELL Part No. 348-247.
R50, R51, R52, R57	1 kΩ, 0.1%, 1/4 W	±15 ppm/°C Resistor, good tolerance, used as part of the analog filter network. These resistors are not soldered, but are plugged into PCB mount sockets for easy modification by the customer. Low drift WELWYN RC55 Series, FARNELL Part No. 339-179.
R53	1 MΩ, 10%, 0.6 W	±50 ppm/°C, FARNELL Part No. 336-660.
R54	100 kΩ, 10%, 1/4 W	±15 ppm/°C, FARNELL Part No. 341-094.
R55, R56	499 Ω, 0.1%, 1/4 W	±15 ppm/°C Resistor, Good Tolerance. Low Drift. FARNELL Part No. 338-886.
C5, C7, C24, C28, C30	10 µF, 10 V dc	Power supply decoupling capacitors, 20%, Philips CW20C 104, FARNELL Part No. 643-579.
C14, C15	22 pF, Ceramic	Gate Oscillator Load Capacitors, FARNELL Part No. 108-927.
C6, C8, C27, C29, C23, C20, C21, C55	100 nF, 50 V	Power Supply Decoupling Capacitors, 10%, X7R type, AVX-KYOCERNA, FARNELL Part No. 146-227.
C9, C10, C11, C12, C13	10 nF	Philips CW15C 103 M, FARNELL Part No. 146-224.
C50, C51, C51, C53, C54	33 nF, 10%, 50 Volt	X7R Capacitor, Part of the Filter Network. These resistors are not soldered, but are plugged into PCB mount sockets for easy modification by the customer. SR15 series AVX-KYOCERNA, FARNELL Part No. 108-948.
U1	AD7751 or AD7755	Supplied by Analog Devices Inc.
U2	74HC08	Quad CMOS AND gates.
U3	AD780	2.5 V Reference, Supplied by Analog Devices Inc.
U4	H11L1	Optical Isolator, by QT, FARNELL Part No. 326-896.
D1, D2, D3	LED	Low Current, Red, FARNELL Part No. 637-087.
Y1	3.579545 MHz	Quartz Crystal, IQD A119C, 50 ppm/°C, FARNELL Part No. 170-229. HC49 Can Style, Pitch 4.88 mm.
SK1, SK3, SK6	Screw Terminal	15 A, 2.5 mm Cable Screw Terminal Sockets. FARNELL Part No. 151-785. Length 10 mm, Pitch 5 mm, Pin diameter 1 mm.
SK2, SK4, SK5	Screw Terminal	15 A, 2.5 mm Cable Screw Terminal Sockets. FARNELL Part No. 151-786. Length 15 mm, Pitch 5 mm, Pin diameter 1 mm.
BNC	BNC Connector	Straight Square, 1.3 mm Holes, 10.2 mm × 10.2 mm. FARNELL Part No. 149-453.

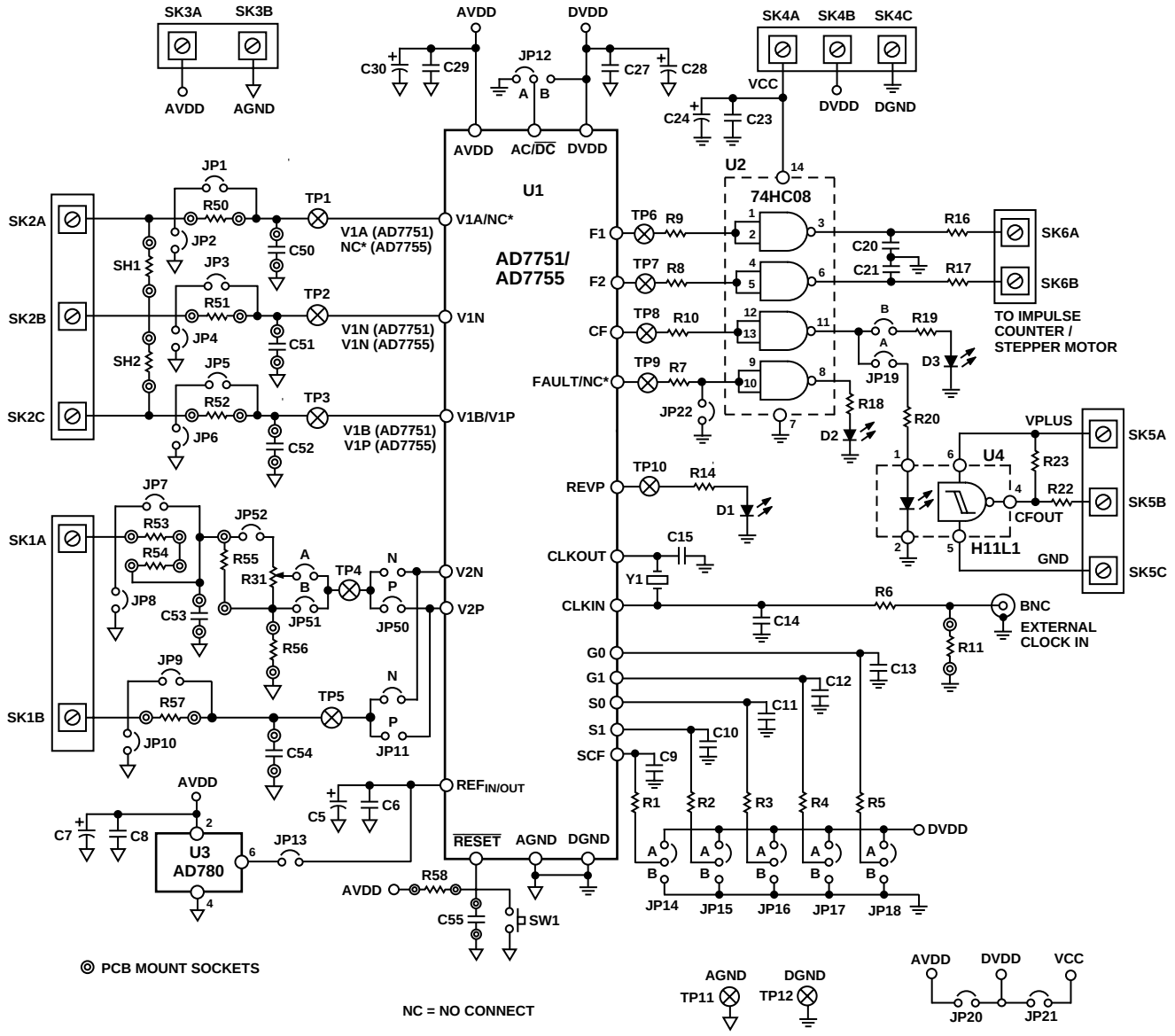


Figure 10. Evaluation Board Schematic

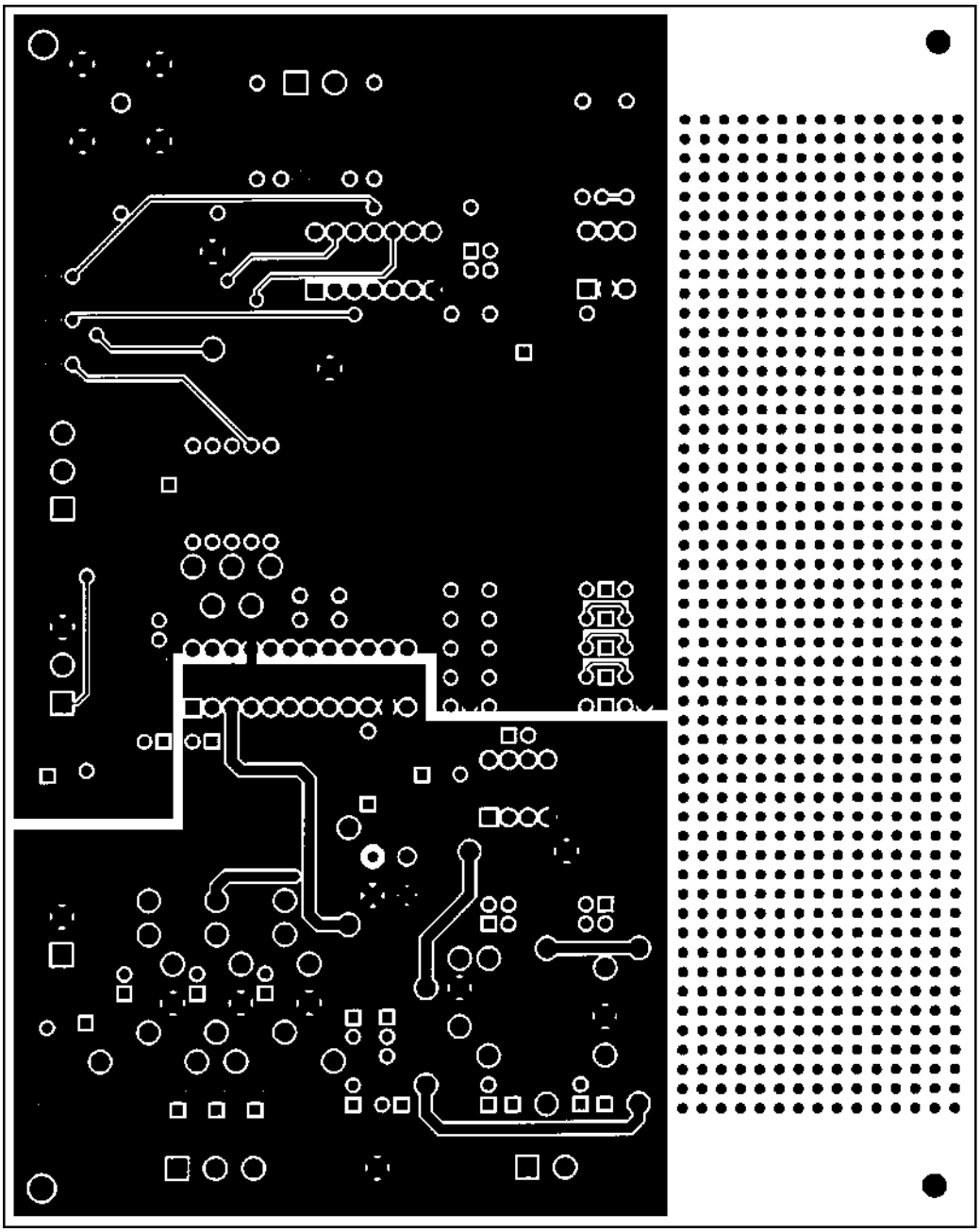


Figure 11. PCB Layout–Component Side

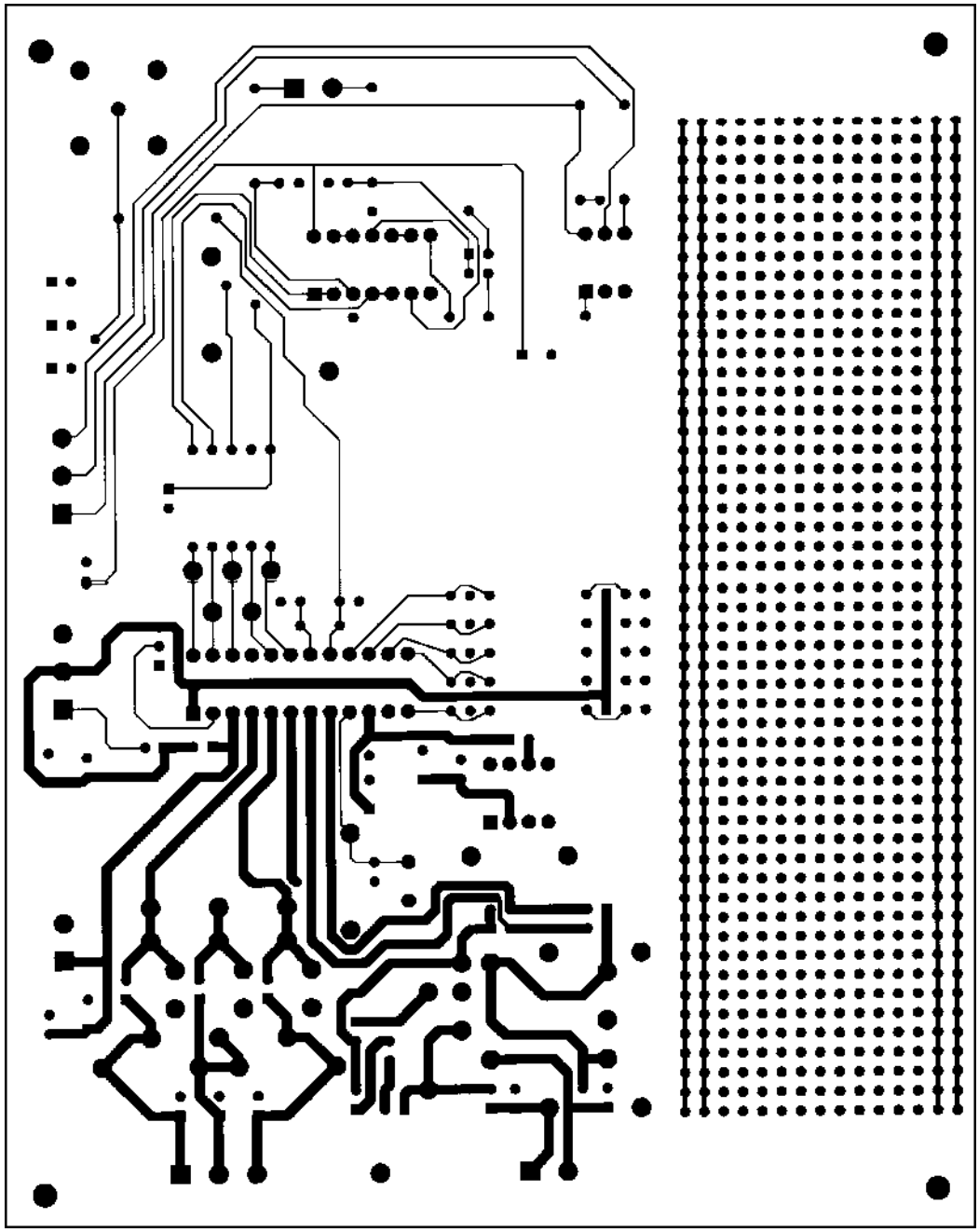


Figure 12. PCB Layout–Solder Side

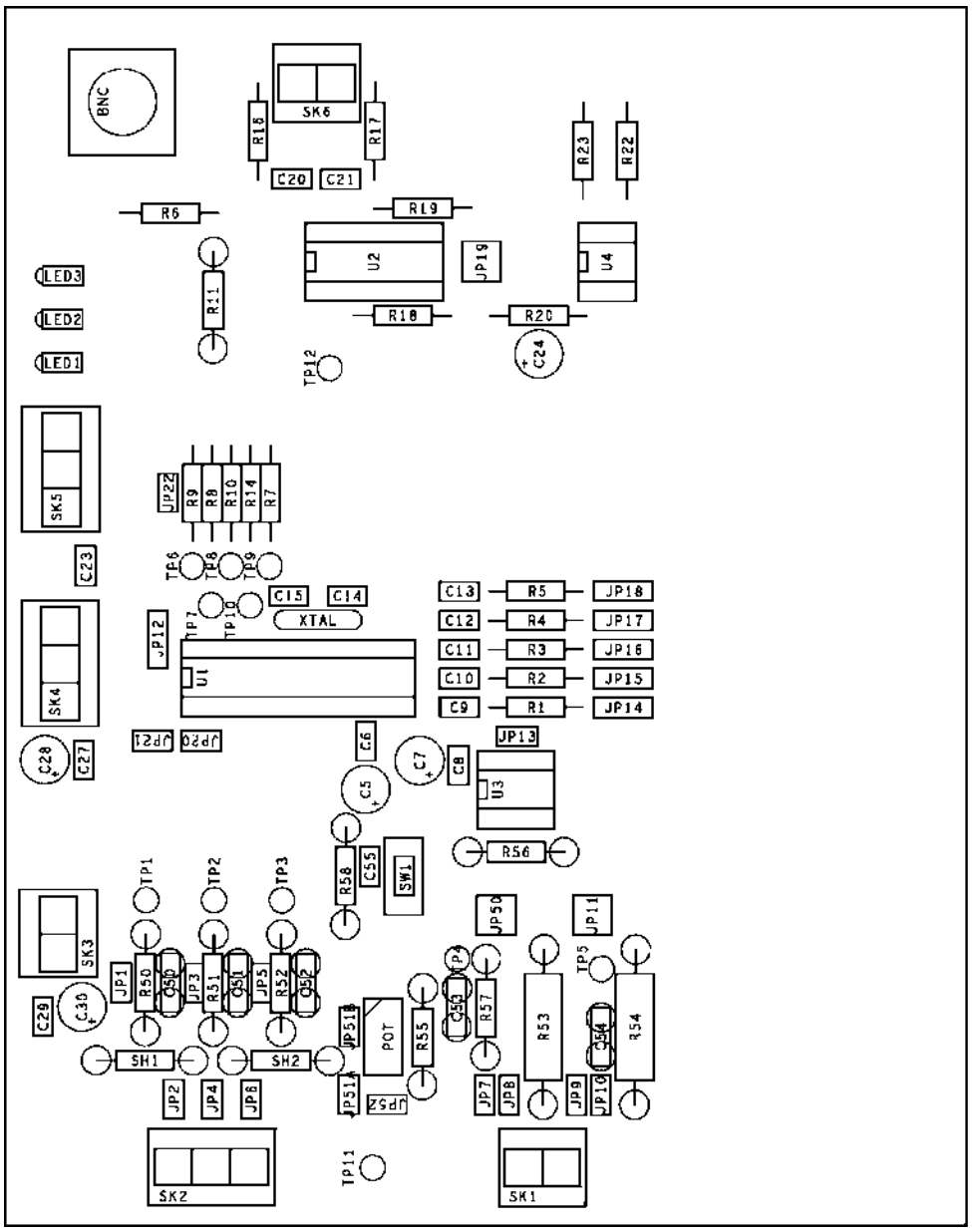


Figure 13. PCB Layout–Component Placement

C3620–2–8/99

PRINTED IN U.S.A.

Energy Metering IC with Pulse Output

ADE7755

FEATURES

High accuracy, surpasses 50 Hz/60 Hz IEC 687/IEC 1036
Less than 0.1% error over a dynamic range of 500 to 1
Supplies active power on the frequency outputs, F1 and F2
High frequency output CF is intended for calibration and supplies instantaneous active power
Synchronous CF and F1/F2 outputs
Logic output REVP provides information regarding the sign of the active power
Direct drive for electromechanical counters and 2-phase stepper motors (F1 and F2)
Programmable gain amplifier (PGA) in the current channel facilitates usage of small shunts and burden resistors
Proprietary ADCs and DSPs provide high accuracy over large variations in environmental conditions and time
On-chip power supply monitoring
On-chip creep protection (no load threshold)
On-chip reference 2.5 V ± 8% (30 ppm/°C typical) with external overdrive capability
Single 5 V supply, low power (15 mW typical)
Low cost CMOS process

GENERAL DESCRIPTION

The ADE7755 is a high accuracy electrical energy measurement IC. The part specifications surpass the accuracy requirements as quoted in the IEC 1036 standard.

The only analog circuitry used in the ADE7755 is in the ADCs and reference circuit. All other signal processing (for example, multiplication and filtering) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

The ADE7755 supplies average active power information on the low frequency outputs, F1 and F2. These logic outputs can be used to directly drive an electromechanical counter or interface to an MCU. The CF logic output gives instantaneous active power information. This output is intended to be used for calibration purposes or for interfacing to an MCU.

The ADE7755 includes a power supply monitoring circuit on the AV_{DD} supply pin. The ADE7755 remains in a reset condition until the supply voltage on AV_{DD} reaches 4 V. If the supply falls below 4 V, the ADE7755 resets and no pulse is issued on F1, F2, and CF.

Internal phase matching circuitry ensures that the voltage and current channels are phase matched whether the HPF in Channel 1 is on or off. An internal no load threshold ensures that the ADE7755 does not exhibit any creep when there is no load.

The ADE7755 is available in a 24-lead SSOP package.

FUNCTIONAL BLOCK DIAGRAM

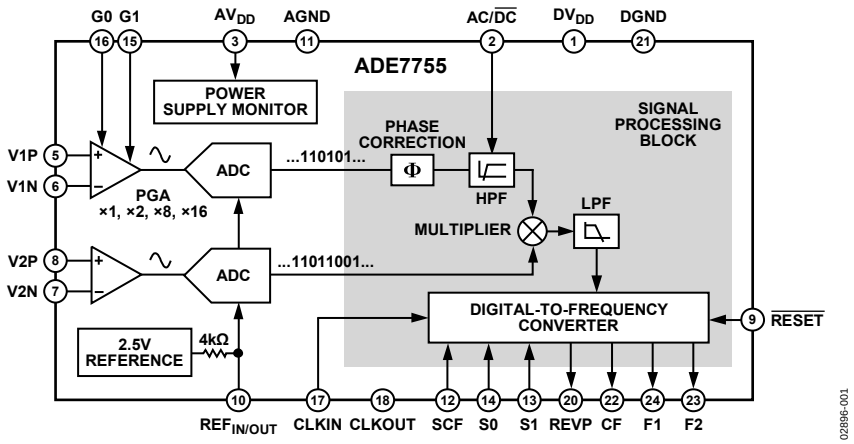


Figure 1.

[1]U.S. Patents 5,745,323; 5,760,617; 5,862,069; and 5,872,469.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

8/09—Rev. 0 to Rev. A

Changes to Format ... Universal
Changes to Features Section and General Description Section ... 1
Moved Figure 2 ... 4
Changes to Pin 22, Pin 23, and Pin 24 Descriptions, Table 4 ... 7
Changes to Terminology Section ... 11
Changes to Theory of Operation Section, Figure 22, Power Factor Considerations Section, and Figure 23 ... 12
Changes to Nonsinusoidal Voltage and Current Section and Analog Inputs Section ... 13
Changes to Figure 27 ... 14
Changes to HPF and Offset Effects Section, Figure 29, and Digital-to-Frequency Conversion Section ... 15
Changes to Figure 32 ... 16
Changes to Transfer Function Section ... 17
Changes to Selecting a Frequency for an Energy Meter Application Section ... 18
Changes to No Load Threshold Section ... 19
Updated Outline Dimensions ... 20
Changes to Ordering Guide ... 20

5/02—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 3.58 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY[1, 2]					
Measurement Error[1] on Channel 1					Channel 2 with full-scale signal (±660 mV), 25°C
Gain = 1		0.1		% reading	Over a dynamic range of 500 to 1
Gain = 2		0.1		% reading	Over a dynamic range of 500 to 1
Gain = 8		0.1		% reading	Over a dynamic range of 500 to 1
Gain = 16		0.1		% reading	Over a dynamic range of 500 to 1
Phase Error[1] Between Channels					Line frequency = 45 Hz to 65 Hz
V1 Phase Lead 37° (PF = 0.8 Capacitive)			±0.1	Degrees	AC/$\overline{DC}$ = 0 and AC/$\overline{DC}$ = 1
V1 Phase Lag 60° (PF = 0.5 Inductive)			±0.1	Degrees	AC/$\overline{DC}$ = 0 and AC/$\overline{DC}$ = 1
AC Power Supply Rejection[1]					AC/$\overline{DC}$ = 1, S0 = S1 = 1, G0 = G1 = 0
Output Frequency Variation (CF)		0.2		% reading	V1 = 100 mV rms, V2 = 100 mV rms @ 50 Hz, ripple on AV_{DD} of 200 mV rms @ 100 Hz
DC Power Supply Rejection[1]					AC/$\overline{DC}$ = 1, S0 = S1 = 1, G0 = G1 = 0
Output Frequency Variation (CF)		±0.3		% reading	V1 = 100 mV rms, V2 = 100 mV rms, AV_{DD} = DV_{DD} = 5 V ± 250 mV
ANALOG INPUTS					See the Analog Inputs section
Maximum Signal Levels			±1	V	V1P, V1N, V2N, and V2P to AGND
Input Impedance (DC)	390			kΩ	CLKIN = 3.58 MHz
−3 dB Bandwidth		14		kHz	CLKIN/256, CLKIN = 3.58 MHz
ADC Offset Error[1, 2]			±25	mV	Gain = 1[1, 2]
Gain Error[1]		±7		% ideal	External 2.5 V reference, gain = 1
					V1 = 470 mV dc, V2 = 660 mV dc
Gain Error Match[1]		±0.2		% ideal	External 2.5 V reference
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range			2.7	V	2.5 V + 8%
	2.3			V	2.5 V − 8%
Input Impedance	3.2			kΩ	
Input Capacitance			10	pF	
ON-CHIP REFERENCE					Nominal 2.5 V
Reference Error			±200	mV	
Temperature Coefficient		±30		ppm/°C	
CLKIN					Note all specifications for CLKIN of 3.58 MHz
Input Clock Frequency			4	MHz	
	1			MHz	
LOGIC INPUTS[3]					
SCF, S0, S1, AC/$\overline{DC}$, $\overline{RESET}$, G0, and G1					
Input High Voltage, V_{INH}	2.4			V	DV_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}			0.8	V	DV_{DD} = 5 V ± 5%
Input Current, I_{IN}			±3	μA	Typically 10 nA, V_{IN} = 0 V to DV_{DD}
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS[3]					
F1 and F2					
Output High Voltage, V_{OH}	4.5			V	I_{SOURCE} = 10 mA, DV_{DD} = 5 V
Output Low Voltage, V_{OL}			0.5	V	I_{SINK} = 10 mA, DV_{DD} = 5 V
CF and REVP					
Output High Voltage, V_{OH}	4			V	I_{SOURCE} = 5 mA, DV_{DD} = 5 V
Output Low Voltage, V_{OL}			0.5	V	I_{SINK} = 5 mA, DV_{DD} = 5 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					For specified performance
AV_{DD}	4.75			V	5 V – 5%
			5.25	V	5 V + 5%
DV_{DD}	4.75			V	5 V – 5%
			5.25	V	5 V + 5%
AI_{DD}			3	mA	Typically 2 mA
DI_{DD}			2.5	mA	Typically 1.5 mA

[1] See the Terminology section.
[2] See the Typical Performance Characteristics section for the plots.
[3] Sample tested during initial release and after any redesign or process change that may affect this parameter.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD} = 5$ V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 3.58 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 2.

Parameter[1, 2]	Specification	Unit	Test Conditions/Comments
t_1[3]	275	ms	F1 and F2 pulse width (logic low)
t_2	See Table 7	sec	Output pulse period; see the Transfer Function section
t_3	1/2 t_2	sec	Time between F1 falling edge and F2 falling edge
t_4[3, 4]	90	ms	CF pulse width (logic high)
t_5	See Table 8	sec	CF pulse period; see the Transfer Function section
t_6	CLKIN/4	sec	Minimum time between F1 and F2 pulse

[1] Sample tested during initial release and after any redesign or process change that may affect this parameter.
[2] See Figure 2.
[3] The pulse widths of F1, F2, and CF are not fixed for higher output frequencies. See the Frequency Outputs section.
[4] The CF pulse is always 18 µs in the high frequency mode. See the Frequency Outputs section and Table 8.

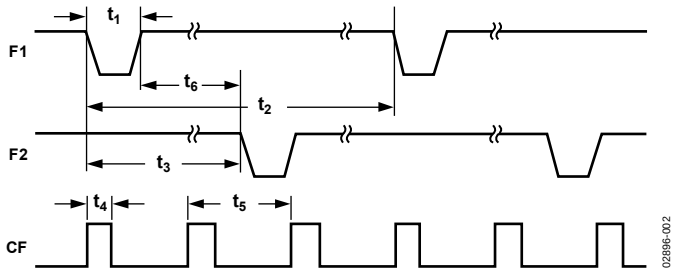


Figure 2. Timing Diagram for Frequency Outputs

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
DV_{DD} to AV_{DD}	−0.3 V to +0.3 V
Analog Input Voltage to AGND	
V1P, V1N, V2P, and V2N	−6 V to +6 V
Reference Input Voltage to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
24-Lead SSOP, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	112°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

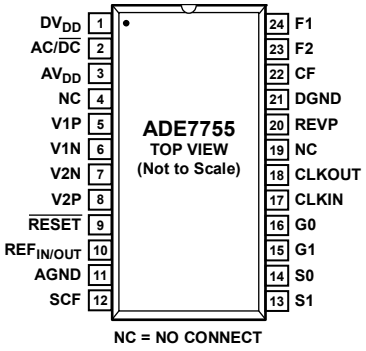


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DV_{DD}	Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7755. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
2	AC/$\overline{DC}$	High-Pass Filter Select. This logic input is used to enable the HPF in Channel 1 (current channel). A Logic 1 on this pin enables the HPF. The associated phase response of this filter is internally compensated over a frequency range of 45 Hz to 1 kHz. The HPF should be enabled in power metering applications.
3	AV_{DD}	Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the ADE7755. The supply should be maintained at 5 V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. This pin should be decoupled to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
4, 19	NC	No Connect.
5, 6	V1P, V1N	Analog Inputs for Channel 1 (Current Channel). These inputs are fully differential voltage inputs with a maximum differential signal level of ±470 mV for specified operation. Channel 1 also has a PGA, and the gain selections are outlined in Table 5. The maximum signal level at these pins is ±1 V with respect to AGND. Both inputs have internal ESD protection circuitry. An overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
7, 8	V2N, V2P	Negative and Positive Inputs for Channel 2 (Voltage Channel). These inputs provide a fully differential input pair with a maximum differential input voltage of ±660 mV for specified operation. The maximum signal level at these pins is ±1 V with respect to AGND. Both inputs have internal ESD protection circuitry, and an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
9	$\overline{RESET}$	Reset Pin. A logic low on this pin holds the ADCs and digital circuitry in a reset condition. Bringing this pin logic low clears the ADE7755 internal registers.
10	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF ceramic capacitor and a 100 nF ceramic capacitor.
11	AGND	This pin provides the ground reference for the analog circuitry in the ADE7755, that is, the ADCs and reference. This pin should be tied to the analog ground plane of the PCB. The analog ground plane is the ground reference for all analog circuitry, for example, antialiasing filters and current and voltage transducers. For good noise suppression, the analog ground plane should be connected to the digital ground plane at one point only. A star ground configuration helps to keep noisy digital currents away from the analog circuits.
12	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output, CF. Table 8 shows how the calibration frequencies are selected.
13, 14	S1, S0	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter. See the Selecting a Frequency for an Energy Meter Application section.
15, 16	G1, G0	These logic inputs are used to select one of four possible gains for Channel 1, that is, V1. The possible gains are 1, 2, 8, and 16. See the Analog Inputs section.

Pin No.	Mnemonic	Description
17	CLKIN	An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7755. The clock frequency for specified operation is 3.579545 MHz. Crystal load capacitance of between 22 pF and 33 pF (ceramic) should be used with the gate oscillator circuit.
18	CLKOUT	A crystal can be connected across this pin and CLKIN to provide a clock source for the ADE7755. The CLKOUT pin can drive one CMOS load when an external clock is supplied at CLKIN or by the gate oscillator circuit.
20	REVP	This logic output goes logic high when negative power is detected, that is, when the phase angle between the voltage and current signals is greater than 90°. This output is not latched and is reset when positive power is detected again. The output goes high or low at the same time that a pulse is issued on CF.
21	DGND	This pin provides the ground reference for digital circuitry in the ADE7755, that is, the multiplier, filters, and digital-to-frequency converter. This pin should be tied to the digital ground plane of the PCB. The digital ground plane is the ground reference for all digital circuitry, for example, counters (mechanical and digital), MCUs, and indicator LEDs. For good noise suppression, the analog ground plane should be connected to the digital ground plane at one point only, for example, a star ground.
22	CF	Calibration Frequency Logic Output. The CF logic output gives instantaneous active power information. This output is intended to be used for calibration purposes. Also, see the SCF pin description.
23, 24	F2, F1	Low Frequency Logic Outputs. F1 and F2 supply average active power information. The logic outputs can be used to directly drive electromechanical counters and 2-phase stepper motors. See the Transfer Function section.

TYPICAL PERFORMANCE CHARACTERISTICS

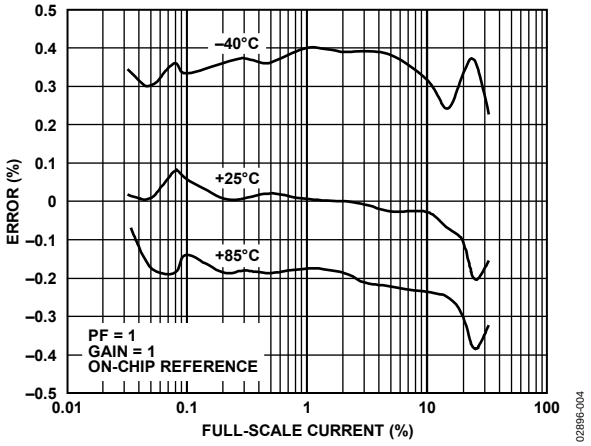


Figure 4. Error as a % of Reading (Gain = 1)

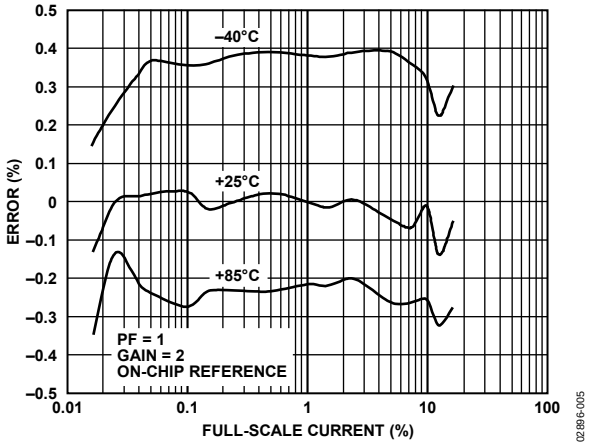


Figure 5. Error as a % of Reading (Gain = 2)

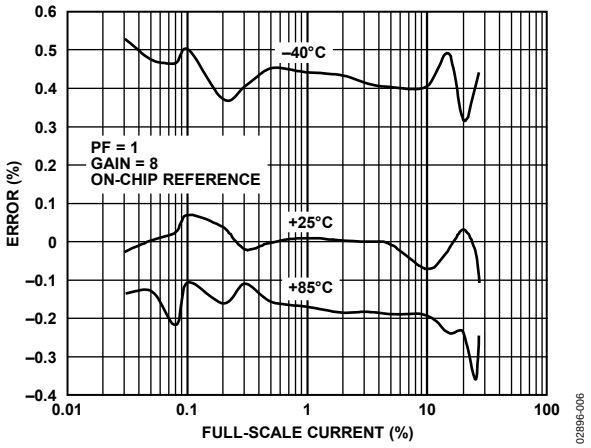


Figure 6. Error as a % of Reading (Gain = 8)

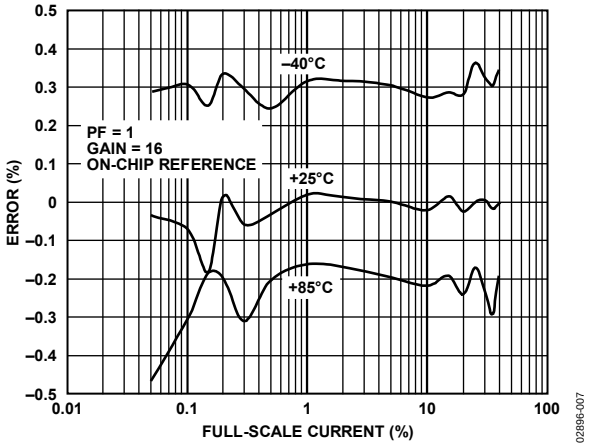


Figure 7. Error as a % of Reading (Gain = 16)

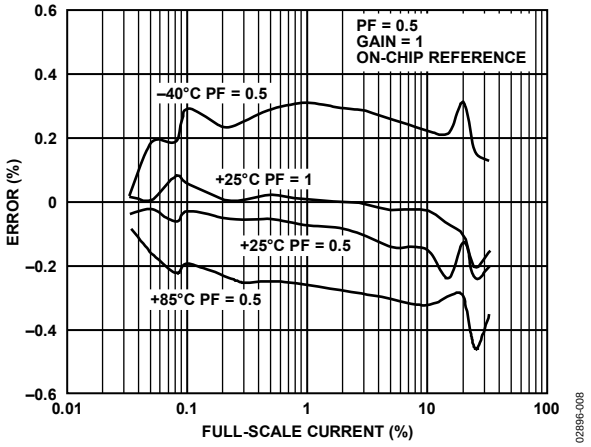


Figure 8. Error as a % of Reading (Gain = 1)

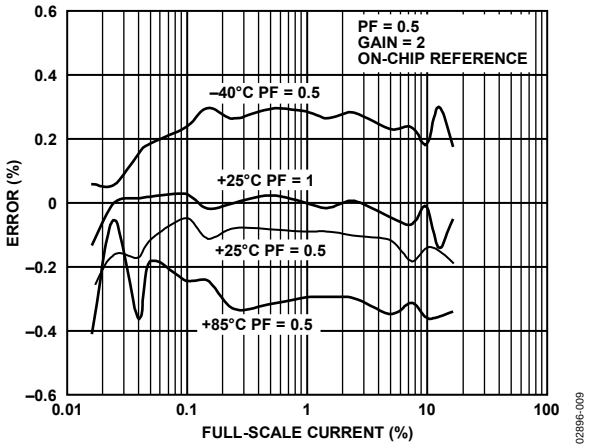


Figure 9. Error as a % of Reading (Gain = 2)

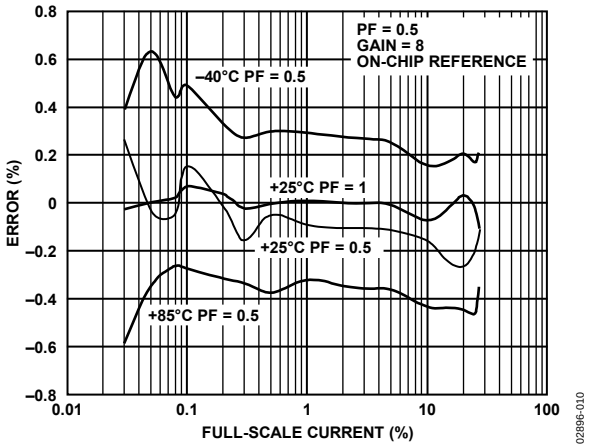


Figure 10. Error as a % of Reading (Gain = 8)

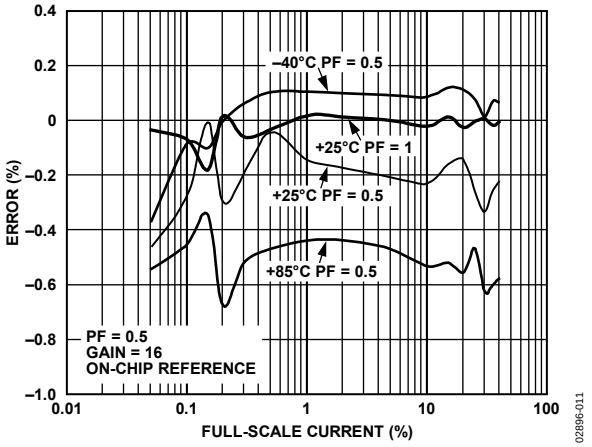


Figure 11. Error as a % of Reading (Gain = 16)

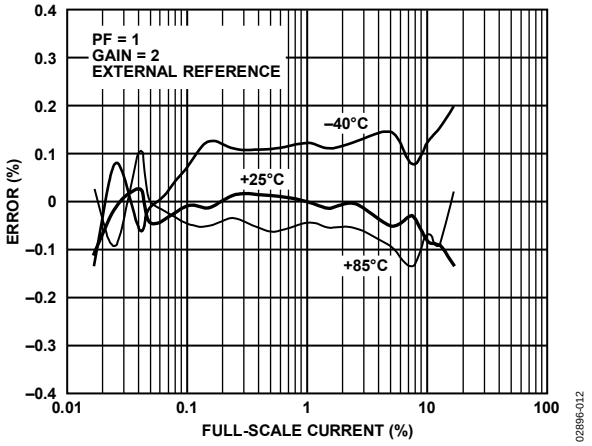


Figure 12. Error as a % of Reading over Temperature with an External Reference (Gain = 2)

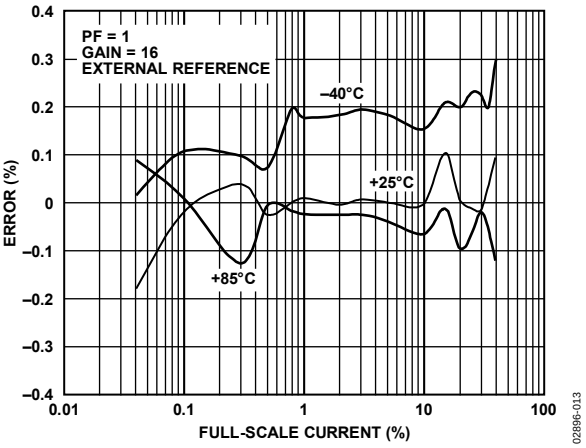


Figure 13. Error as a % of Reading over Temperature with an External Reference (Gain = 16)

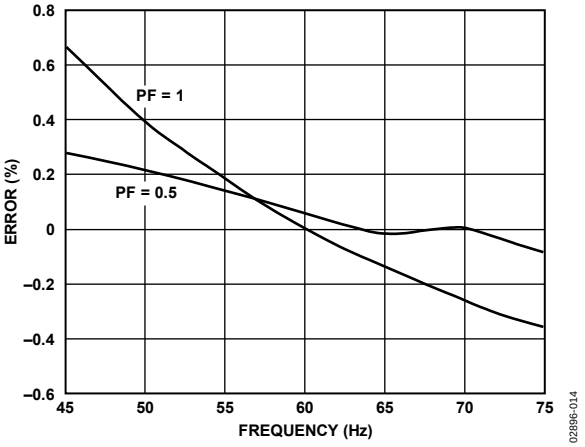


Figure 14. Error as a % of Reading over Frequency

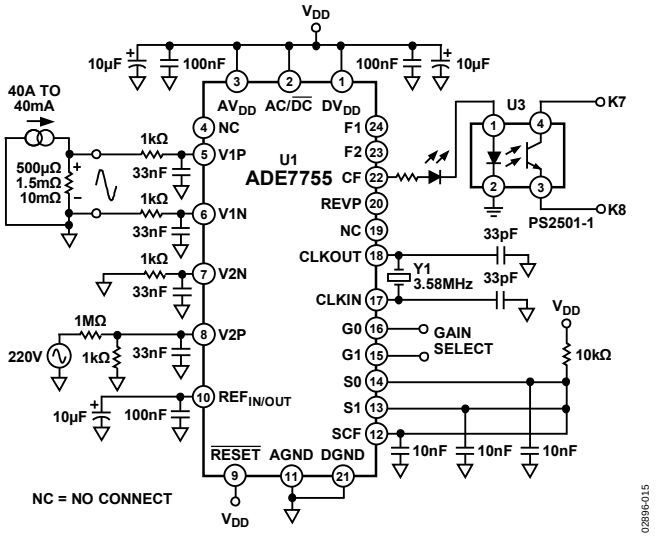


Figure 15. Test Circuit for Performance Curves

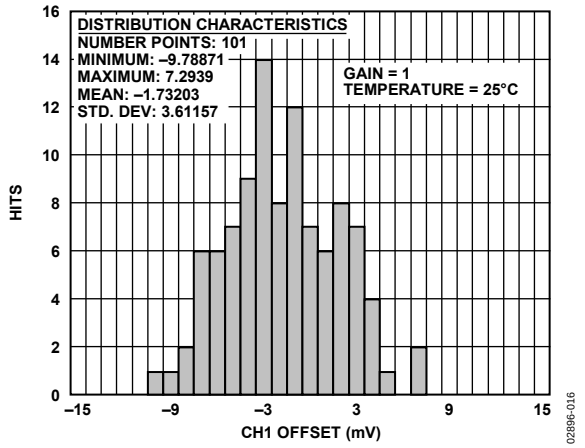


Figure 16. Channel 1 Offset Distribution (Gain = 1)

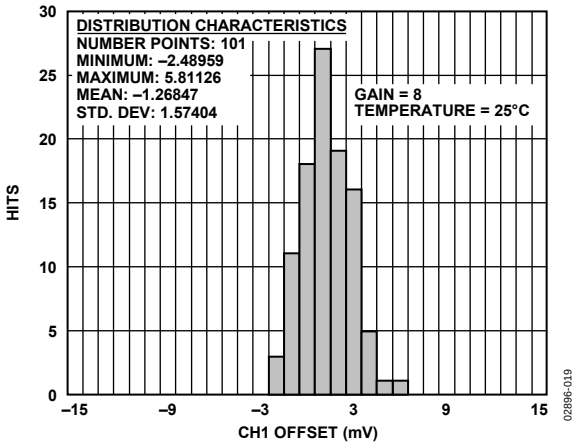


Figure 19. Channel 1 Offset Distribution (Gain = 8)

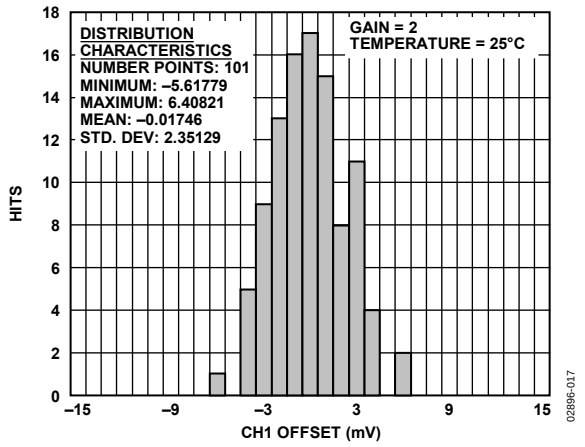


Figure 17. Channel 1 Offset Distribution (Gain = 2)

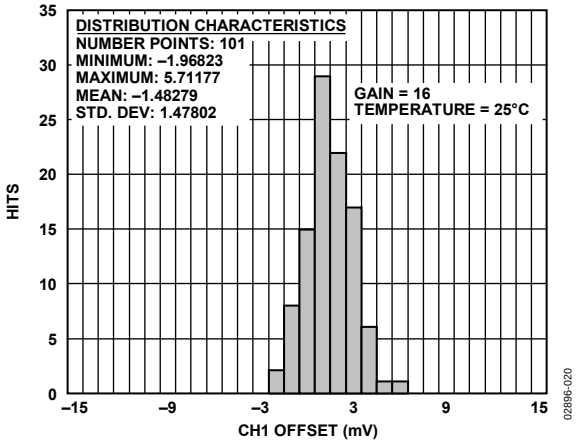


Figure 20. Channel 1 Offset Distribution (Gain = 16)

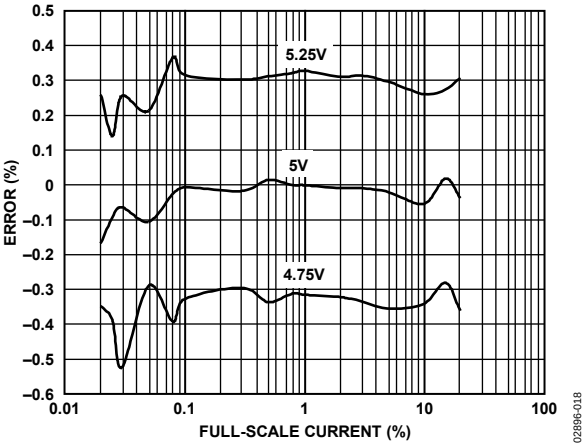


Figure 18. PSR with Internal Reference (Gain = 16)

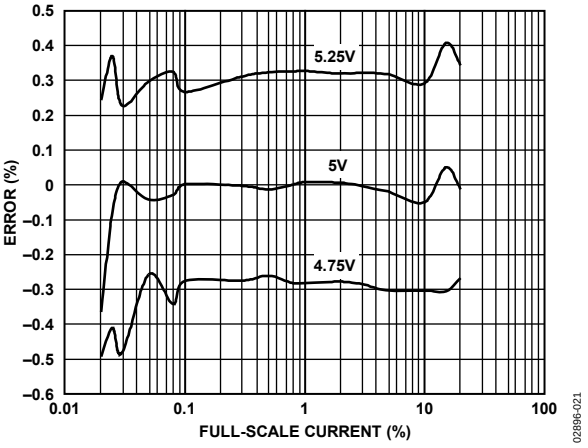


Figure 21. PSR with External Reference (Gain = 16)

TERMINOLOGY

Measurement Error
The error associated with the energy measurement made by the ADE7755 is defined by the following formula:

$$Percentage\,Error = \frac{Energy\,Registered\,by\,the\,ADE7755 - True\,Energy}{True\,Energy} \times 100\%$$

Phase Error Between Channels
The high-pass filter (HPF) in Channel 1 has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase compensation network is also placed in Channel 1. The phase compensation network matches the phase to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range of 40 Hz to 1 kHz. See Figure 30 and Figure 31.

Power Supply Rejection (PSR)
The PSR quantifies the ADE7755 measurement error as a percentage of the reading when the power supplies are varied.

For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A 200 mV rms/100 Hz signal is then introduced onto the supplies and a second reading is obtained under the same input signal levels. Any error introduced is expressed as a percentage of the reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. The supplies are then varied ±5% and a second reading is obtained with the same input signal levels. Any error introduced is again expressed as a percentage of the reading.

ADC Offset Error
The ADC offset error refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a small dc signal (offset). The offset decreases with increasing gain in Channel 1. This specification is measured at a gain of 1. At a gain of 16, the dc offset is typically less than 1 mV. However, when the HPF is switched on, the offset is removed from the current channel, and the power calculation is not affected by this offset.

Gain Error
The gain error of the ADE7755 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. It is measured with a gain of 1 in Channel 1. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7755 transfer function (see the Transfer Function section).

Gain Error Match
The gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1 and a gain of 2, 8, or 16. It is expressed as a percentage of the output frequency obtained under a gain of 1. This gives the gain error observed when the gain selection is changed from 1 to 2, 8, or 16.

THEORY OF OPERATION

The two ADCs of the ADE7755 digitize the voltage signals from the current and voltage transducers. These ADCs are 16-bit, second-order Σ-Δ with an oversampling rate of 900 kHz. This analog input structure greatly simplifies transducer interfacing by providing a wide dynamic range for direct connection to the transducer and also by simplifying the antialiasing filter design. A programmable gain stage in the current channel further facilitates easy transducer interfacing. A high-pass filter in the current channel removes any dc components from the current signal. This removal eliminates any inaccuracies in the active power calculation due to offsets in the voltage or current signals (see the HPF and Offset Effects section).

The active power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. To extract the active power component (that is, the dc component), the instantaneous power signal is low-pass filtered. Figure 22 illustrates the instantaneous active power signal and shows how the active power information can be extracted by low-pass filtering the instantaneous power signal. This scheme correctly calculates active power for nonsinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

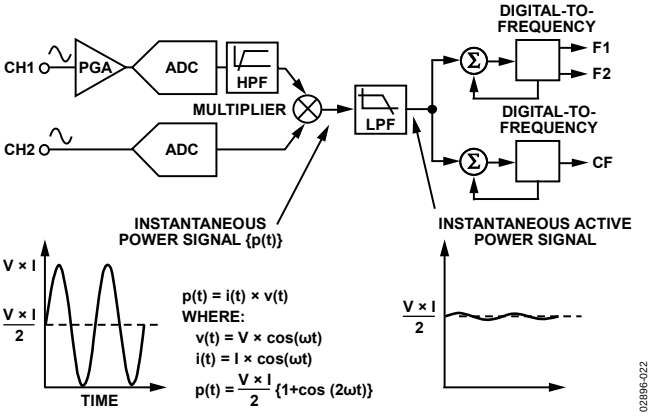


Figure 22. Signal Processing Block Diagram

The low frequency output of the ADE7755 is generated by accumulating this active power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average active power. This average active power information can, in turn, be accumulated (for example, by a counter) to generate active energy information. Because of its high output frequency and shorter integration time, the calibration frequency (CF) output is proportional to the instantaneous active power. This is useful for system calibration purposes that take place under steady load conditions.

POWER FACTOR CONSIDERATIONS

The method used to extract the active power information from the instantaneous power signal (that is, by low-pass filtering) is valid even when the voltage and current signals are not in phase. Figure 23 displays the unity power factor condition and a displacement power factor (DPF) = 0.5, that is, current signal lagging the voltage by 60°. Assuming that the voltage and current waveforms are sinusoidal, the active power component of the instantaneous power signal (that is, the dc term) is given by

$$\left(\frac{V \times I}{2}\right) \times \cos(60°)$$

This is the correct active power calculation.

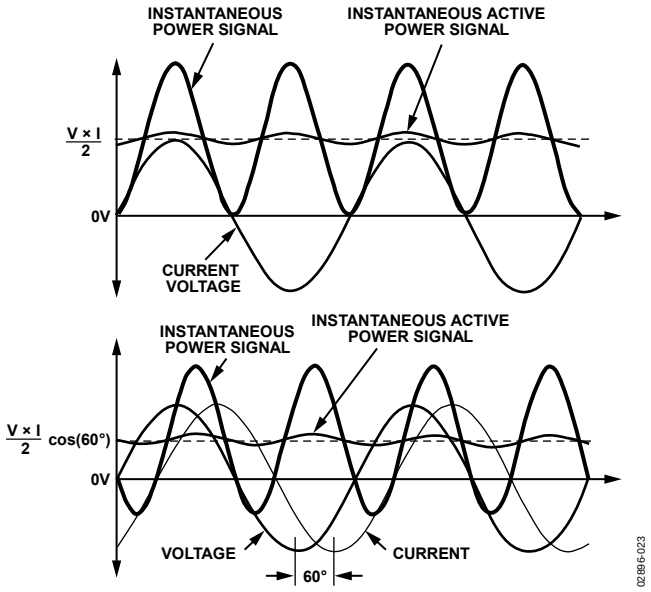


Figure 23. DC Component of Instantaneous Power Signal Conveys Active Power Information PF < 1

NONSINUSOIDAL VOLTAGE AND CURRENT

The active power calculation method also holds true for non-sinusoidal current and voltage waveforms. All voltage and current waveforms in practical applications have some harmonic content. Using the Fourier Transform operation, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content.

$$v(t) = V_O + \sqrt{2} \times \sum_{h \neq 0}^{\infty} V_h \times \sin\left(h\omega t + a_h\right) \quad (1)$$

where:
$v(t)$ is the instantaneous voltage.
V_O is the average voltage value.
V_h is the rms value of the voltage harmonic, h.
a_h is the phase angle of the voltage harmonic.

$$i(t) = I_O + \sqrt{2} \times \sum_{h \neq 0}^{\infty} I_h \times \sin(h\omega t + \beta_h) \quad (2)$$

where:
$i(t)$ is the instantaneous current.
I_O is the current dc component.
I_h is the rms value of the current harmonic, h.
β_h is the phase angle of the current harmonic.

Using Equation 1 and Equation 2, the active power (P) can be expressed in terms of its fundamental active power (P1) and harmonic active power (P_H).

$$P = P_1 + P_H \quad (3)$$

where:
P_1 is the active power of the fundamental component:

$$P_1 = V_1 \times I_1 \cos\Phi_1$$
$$\Phi_1 = \alpha_1 - \beta_1$$

and

P_H is the active power of all harmonic components:

$$P_H = \sum_{h \neq 1}^{\infty} V_h \times I_h \cos\Phi_h$$

$$\Phi_h = \alpha_h - \beta_h$$

A harmonic active power component is generated for every harmonic, provided that the harmonic is present in both the voltage and current waveforms. The power factor calculation previously shown is accurate in the case of a pure sinusoid; therefore, the harmonic active power must also correctly account for the power factor because it is made up of a series of pure sinusoids.

Note that the input bandwidth of the analog inputs is 14 kHz with a master clock frequency of 3.5795 MHz.

ANALOG INPUTS

Channel 1 (Current Channel)

The voltage output from the current transducer is connected to the ADE7755 at Channel 1. Channel 1 is a fully differential voltage input. V1P is the positive input with respect to V1N.

The maximum peak differential signal on Channel 1 should be less than ±470 mV (330 mV rms for a pure sinusoidal signal) for specified operation. Note that Channel 1 has a programmable gain amplifier (PGA) with user-selectable gain of 1, 2, 8, or 16 (see Table 5). These gains facilitate easy transducer interfacing.

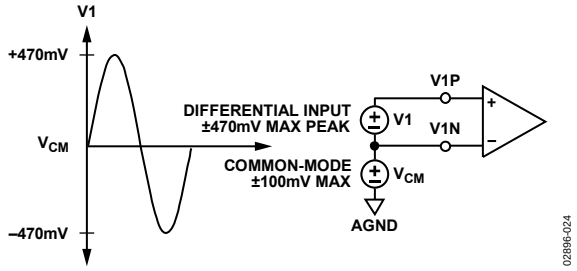


Figure 24. Maximum Signal Levels, Channel 1, Gain = 1

Figure 24 illustrates the maximum signal levels on V1P and V1N. The maximum differential voltage is ±470 mV divided by the gain selection. The differential voltage signal on the inputs must be referenced to a common mode, for example, AGND. The maximum common-mode signal is ±100 mV, as shown in Figure 24.

Table 5. Gain Selection for Channel 1

G1	G0	Gain	Maximum Differential Signal (mV)
0	0	1	±470
0	1	2	±235
1	0	8	±60
1	1	16	±30

Channel 2 (Voltage Channel)

The output of the line voltage transducer is connected to the ADE7755 at this analog input. Channel 2 is a fully differential voltage input. The maximum peak differential signal on Channel 2 is ±660 mV. Figure 25 illustrates the maximum signal levels that can be connected to Channel 2 of the ADE7755.

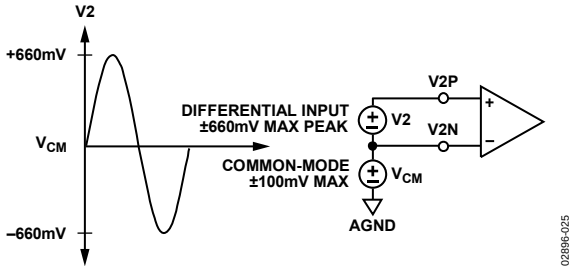


Figure 25. Maximum Signal Levels, Channel 2

Channel 2 must be driven from a common-mode voltage, that is, the differential voltage signal on the input must be referenced to a common mode (usually AGND). The analog inputs of the ADE7755 can be driven with common-mode voltages of up to 100 mV with respect to AGND. However, best results are achieved using a common mode equal to AGND.

TYPICAL CONNECTION DIAGRAMS

Figure 26 shows a typical connection diagram for Channel 1. A current transformer (CT) is the current transducer selected for this example. Note that the common-mode voltage for Channel 1 is AGND and is derived by center-tapping the burden resistor to AGND. This provides the complementary analog input signals for V1P and V1N. The CT turns ratio and burden resistor Rb are selected to give a peak differential voltage of ±470 mV/gain at maximum load.

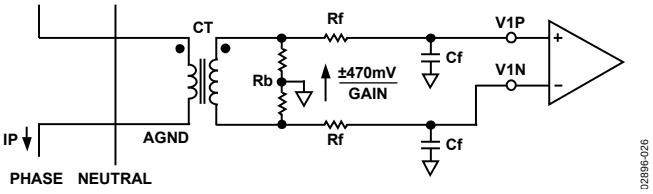


Figure 26. Typical Connection for Channel 1

Figure 27 shows two typical connections for Channel 2. The first option uses a potential transformer (PT) to provide complete isolation from the power line. In the second option, the ADE7755 is biased around the neutral wire, and a resistor divider provides a voltage signal that is proportional to the line voltage. Adjusting the ratio of Ra, Rb, and VR is also a convenient way of carrying out a gain calibration on the meter.

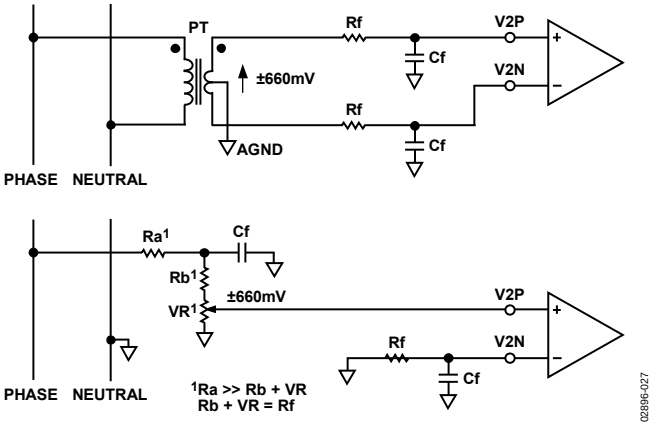


Figure 27. Typical Connections for Channel 2

POWER SUPPLY MONITOR

The ADE7755 contains an on-chip power supply monitor. The analog supply (AV_{DD}) is continuously monitored by the ADE7755. If the supply is less than 4 V ± 5%, the ADE7755 resets. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built-in hysteresis and filtering. These features give a high degree of immunity to false triggering due to noisy supplies.

In Figure 28, the trigger level is nominally set at 4 V. The tolerance on this trigger level is about ±5%. The power supply and decoupling for the part should be such that the ripple at AV_{DD} does not exceed 5 V ± 5%, as specified for normal operation.

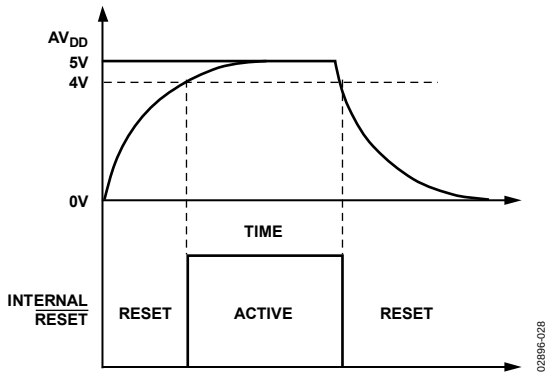


Figure 28. On-Chip Power Supply Monitor

HPF and Offset Effects

Figure 29 shows the effect of offsets on the active power calculation. An offset on Channel 1 and Channel 2 contributes a dc component after multiplication. Because the dc component is extracted by the LPF, it accumulates as active power. If not properly filtered, dc offsets introduce error to the energy accumulation. This problem is easily avoided by enabling the HPF (that is, the AC/$\overline{\text{DC}}$ pin is set to logic high) in Channel 1. By removing the offset from at least one channel, no error component can be generated at dc by the multiplication. Error terms at cos(ωt) are removed by the LPF and the digital-to-frequency conversion (see the Digital-to-Frequency Conversion section).

$$\{V\cos(\omega t) + V_{OS}\} \times \{I\cos(\omega t) + I_{OS}\} =$$

$$\frac{V \times I}{2} + V_{OS} \times I_{OS} + V_{OS} \times I\cos(\omega t) + I_{OS} \times V\cos(\omega t) +$$

$$\frac{V \times I}{2} \times \cos(2\omega t)$$

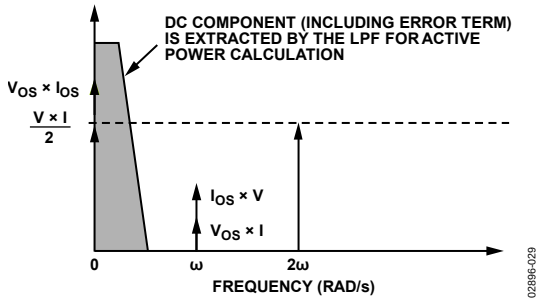


Figure 29. Effect of Channel Offset on the Active Power Calculation

The HPF in Channel 1 has an associated phase response that is compensated for on chip. The phase compensation is activated when the HPF is enabled and is disabled when the HPF is not activated. Figure 30 and Figure 31 show the phase error between channels with the compensation network activated. The ADE7755 is phase compensated up to 1 kHz, as shown. This ensures correct active harmonic power calculation even at low power factors.

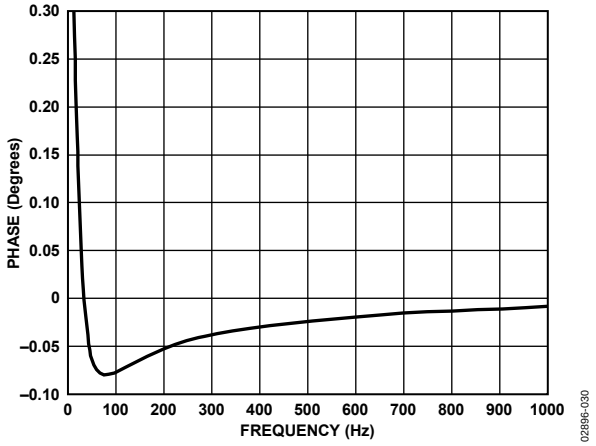


Figure 30. Phase Error Between Channels (0 Hz to 1 kHz)

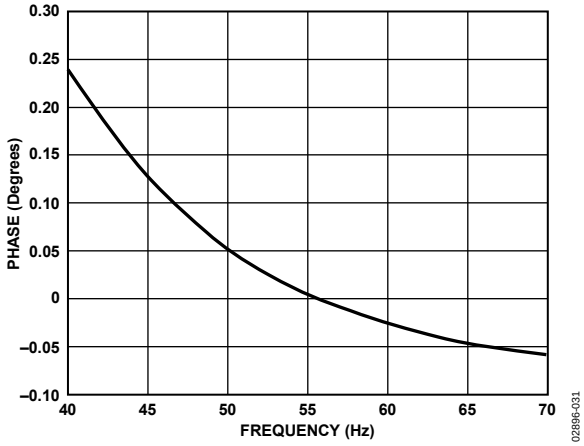


Figure 31. Phase Error Between Channels (40 Hz to 70 Hz)

DIGITAL-TO-FREQUENCY CONVERSION

The digital output of the low-pass filter after multiplication contains the active power information. However, because this LPF is not an ideal brick-wall filter implementation, the output signal also contains attenuated components at the line frequency and its harmonics, that is, cos(hωt) where h = 1, 2, 3, and so on.

The magnitude response of the filter is given by

$$|H(f)| = \frac{1}{1 + (f/8.9\,\text{Hz})} \quad (4)$$

For a line frequency of 50 Hz, the filter gives an attenuation of the 2ω (100 Hz) component of approximately −22 dB. The dominating harmonic is at twice the line frequency, that is, cos(2 ωt), which is due to the instantaneous power signal.

Figure 32 shows the instantaneous active power signal at the output of the LPF, which still contains a significant amount of instantaneous power information, that is, cos(2 ωt). This signal is then passed to the digital-to-frequency converter where it is integrated (accumulated) over time to produce an output frequency. This accumulation of the signal suppresses or averages out any non-dc components in the instantaneous active power signal. The average value of a sinusoidal signal is 0. Therefore, the frequency generated by the ADE7755 is proportional to the average active power. Figure 32 shows the digital-to-frequency conversion for steady load conditions, that is, constant voltage and current.

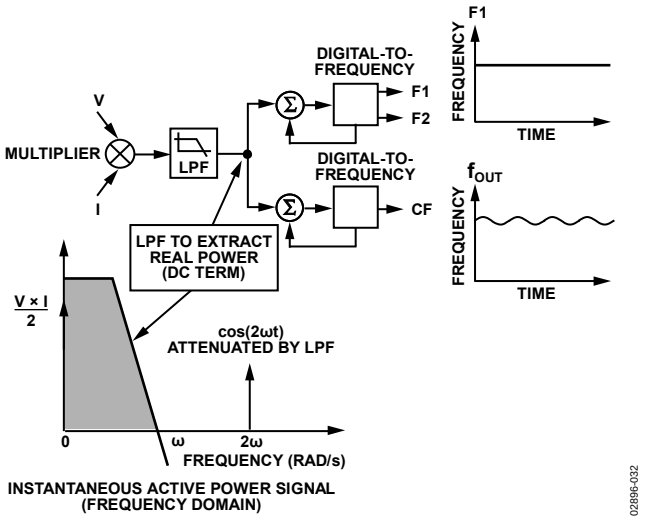


Figure 32. Active Power-to-Frequency Conversion

As can be seen in Figure 32, the frequency output CF varies over time, even under steady load conditions. This frequency variation is primarily due to the cos(2 ωt) component in the instantaneous active power signal. The output frequency on CF can be up to 2048 times higher than the frequency on F1 and F2. This higher output frequency is generated by accumulating the instantaneous active power signal over a much shorter time while converting it to a frequency. This shorter accumulation period means less averaging of the cos(2 ωt) component. Consequently, some of this instantaneous power signal passes through the digital-to-frequency conversion, which is not a problem in the application. When CF is used for calibration purposes, the frequency should be averaged by the frequency counter. This averaging operation removes any ripple. If CF is measuring energy, for example, in a microprocessor-based application, the CF output should also be averaged to calculate power. Because the outputs, F1 and F2, operate at a much lower frequency, more averaging of the instantaneous active power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple-free frequency output.

INTERFACING THE ADE7755 TO A MICROCONTROLLER FOR ENERGY MEASUREMENT

The easiest way to interface the ADE7755 to a microcontroller is to use the CF high frequency output with the output frequency scaling set to 2048 × F1, F2. This is done by setting SCF = 0 and S0 = S1 = 1 (see Table 8). With full-scale ac signals on the analog inputs, the output frequency on CF is approximately 5.5 kHz. Figure 33 illustrates one scheme that can be used to digitize the output frequency and carry out the necessary averaging described in the Digital-to-Frequency Conversion section.

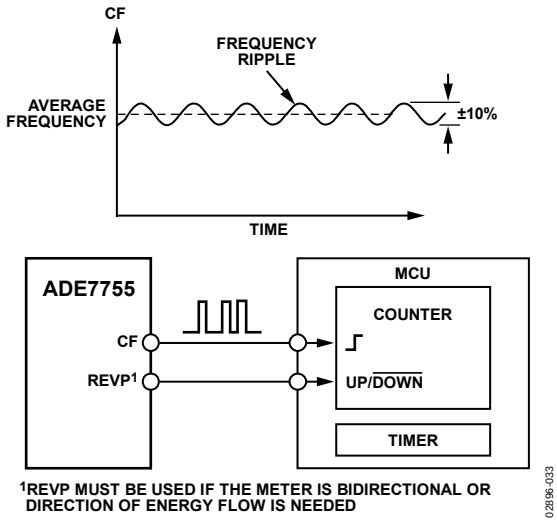


Figure 33. Interfacing the ADE7755 to an MCU

As shown in Figure 33, the frequency output CF is connected to an MCU counter or port, which counts the number of pulses in a given integration time that is determined by an MCU internal timer. The average power proportional to the average frequency is given by

$$Average\ Frequency = Average\ Active\ Power = \frac{Counter}{Timer}$$

The energy consumed during an integration period is given by

$$Energy = Average\ Power \times Time = \frac{Counter}{Time} \times Time = Counter$$

For the purpose of calibration, this integration time can be 10 seconds to 20 seconds to accumulate enough pulses to ensure correct averaging of the frequency. In normal operation, the integration time can be reduced to 1 second or 2 seconds depending, for example, on the required update rate of a display. With shorter integration times on the MCU, the amount of energy in each update may still have some small amount of ripple, even under steady load conditions. However, over a minute or more, the measured energy has no ripple.

POWER MEASUREMENT CONSIDERATIONS

Calculating and displaying power information always has some associated ripple that depends on the integration period used in the MCU to determine average power and also the load. For example, at light loads, the output frequency can be 10 Hz. With an integration period of 2 seconds, only about 20 pulses are counted. The possibility of missing one pulse always exists because the ADE7755 output frequency is running asynchronously to the MCU timer. This possibility results in a 1-in-20 (or 5%) error in the power measurement.

TRANSFER FUNCTION

Frequency Outputs F1 and F2

The ADE7755 calculates the product of two voltage signals (on Channel 1 and Channel 2) and then low-pass filters this product to extract active power information. This active power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low, for example, 0.34 Hz maximum for ac signals with S0 = S1 = 0 (see Table 7). This means that the frequency at these outputs is generated from active power information accumulated over a relatively long time. The result is an output frequency that is proportional to the average active power. The averaging of the active power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation:

$$Freq = \frac{8.06 \times V1 \times V2 \times Gain \times f_i}{V_{REF}{}^2}$$

where:
Freq = output frequency on F1 and F2 (Hz).
V1 = differential rms voltage signal on Channel 1 (volts).
V2 = differential rms voltage signal on Channel 2 (volts).
Gain = 1, 2, 8, or 16, depending on the PGA gain selection made using logic inputs G0 and G1.
V_{REF} = the reference voltage (2.5 V ± 8%) (volts).
f_i = one of the four possible frequencies (f_1, f_2, f_3, or f_4) selected by using the logic inputs S0 and S1, see Table 6.

Table 6. f_1, f_2, f_3, and f_4 Frequency Selection

S1	S0	f_1, f_2, f_3, and f_4 (Hz)	XTAL/CLKIN[1]
0	0	f_1 = 1.7	3.579 MHz/2^{21}
0	1	f_2 = 3.4	3.579 MHz/2^{20}
1	0	f_3 = 6.8	3.579 MHz/2^{19}
1	1	f_4 = 13.6	3.579 MHz/2^{18}

[1] f_1, f_2, f_3, or f_4 is a binary fraction of the master clock and, therefore, varies if the specified CLKIN frequency is altered.

Example 1

If full-scale differential dc voltages of +470 mV and −660 mV are applied to V1 and V2, respectively (470 mV is the maximum differential voltage that can be connected to Channel 1, and 660 mV is the maximum differential voltage that can be connected to Channel 2), the expected output frequency is calculated as follows:

$$Freq = \frac{8.06 \times V1 \times V2 \times Gain \times f_i}{V_{REF}{}^2}$$

where:
Gain = 1, G0 = G1 = 0.
f_i = f_1 = 1.7 Hz, S0 = S1 = 0.
V1 = +470 mV dc = 0.47 V (rms of dc = dc).
V2 = −660 mV dc = 0.66 V (rms of dc = |dc|).
V_{REF} = 2.5 V (nominal reference value).

If the on-chip reference is used, actual output frequencies may vary from device to device due to a reference tolerance of ±8%.

Example 2

In this example, with ac voltages of ±470 mV peak applied to V1 and ±660 mV peak applied to V2, the expected output frequency is calculated as follows:

$$Freq = \frac{8.06 \times 0.47 \times 0.66 \times 1 \times 1.7}{\sqrt{2} \times \sqrt{2} \times 2.5^2} = 0.34$$

where:
Gain = 1, G0 = G1 = 0.
f_i = f_1 = 1.7 Hz, S0 = S1 = 0.
V1 = rms of 470 mV peak ac = 0.47/√2 V.
V2 = rms of 660 mV peak ac = 0.66/√2 V.
V_{REF} = 2.5 V (nominal reference value).

If the on-chip reference is used, actual output frequencies may vary from device to device due to a reference tolerance of ±8%.

As can be seen from these two example calculations, the maximum output frequency for ac inputs is always half that for dc input signals. Table 7 shows a complete listing of all the maximum output frequencies.

Table 7. Maximum Output Frequency on F1 and F2

S1	S0	Maximum Frequency for DC Inputs (Hz)	Maximum Frequency for AC Inputs (Hz)
0	0	0.68	0.34
0	1	1.36	0.68
1	0	2.72	1.36
1	1	5.44	2.72

Frequency Output CF

The pulse output CF is intended for use during calibration. The output pulse rate on CF can be up to 2048 times the pulse rate on F1 and F2. The lower the f_i frequency selected (i = 1, 2, 3, or 4), the higher the CF scaling (except for the high frequency mode SCF = 0, S1 = S0 = 1). Table 8 shows how the two frequencies are related, depending on the state of the logic inputs, S0, S1, and SCF. Because of its relatively high pulse rate, the frequency at CF is proportional to the instantaneous active power. As is the case with F1 and F2, the frequency is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this active power information is accumulated over a much shorter time. Therefore, less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the active power signal, the CF output is much more responsive to power fluctuations (see the signal processing block diagram in Figure 22).

Table 8. Maximum Output Frequency on CF

SCF	S1	S0	f_1, f_2, f_3, and f_4 (Hz)	CF Maximum for AC Signals
1	0	0	f_1 = 1.7	128 × F1, F2 = 43.52 Hz
0	0	0	f_1 = 1.7	64 × F1, F2 = 21.76 Hz
1	0	1	f_2 = 3.4	64 × F1, F2 = 43.52 Hz
0	0	1	f_2 = 3.4	32 × F1, F2 = 21.76 Hz
1	1	0	f_3 = 6.8	32 × F1, F2 = 43.52 Hz
0	1	0	f_3 = 6.8	16 × F1, F2 = 21.76 Hz
1	1	1	f_4 = 13.6	16 × F1, F2 = 43.52 Hz
0	1	1	f_4 = 13.6	2048 × F1, F2 = 5.57 kHz

SELECTING A FREQUENCY FOR AN ENERGY METER APPLICATION

As shown in Table 6, the user can select one of four frequencies. This frequency selection determines the maximum frequency on F1 and F2. These outputs are intended to be used to drive the energy register (electromechanical or other). Because only four different output frequencies can be selected, the available frequency selection has been optimized for a meter constant of 100 imp/kWh with a maximum current between 10 A and 120 A. Table 9 shows the output frequency for several maximum currents (I_{MAX}) with a line voltage of 220 V. In all cases, the meter constant is 100 imp/kWh.

Table 9. F1 and F2 Frequency at 100 imp/kWh

I_{MAX} (A)	F1 and F2 (Hz)
12.5	0.076
25	0.153
40	0.244
60	0.367
80	0.489
120	0.733

The f_i frequencies (i = 1, 2, 3, or 4) allow complete coverage of this range of output frequencies on F1 and F2. When designing an energy meter, the nominal design voltage on Channel 2 (voltage) should be set to half scale to allow for calibration of the meter constant. The current channel should also be no more than half scale when the meter sees maximum load. This allows overcurrent signals and signals with high crest factors to be accommodated. Table 10 shows the output frequency on F1 and F2 when both analog inputs are half scale. The frequencies listed in Table 10 align well with those listed in Table 9 for maximum load.

Table 10. F1 and F2 Frequency with Half-Scale AC Inputs

S1	S0	f_1, f_2, f_3, and f_4 (Hz)	F1 and F2 Frequency on CH1 and CH2 Half-Scale AC Inputs (Hz)
0	0	f_1 = 1.7	0.085
0	1	f_2 = 3.4	0.17
1	0	f_3 = 6.8	0.34
1	1	f_4 = 13.6	0.68

When selecting a suitable f_i frequency (i = 1, 2, 3, or 4) for a meter design, the frequency output at I_{MAX} (maximum load) with a meter constant of 100 imp/kWh should be compared with Column 4 of Table 10. The frequency that is closest in Table 10 determines the best choice of f_i frequency (i = 1, 2, 3, or 4). For example, if a meter with a maximum current of 25 A is being designed, the output frequency on F1 and F2 with a meter constant of 100 imp/kWh is 0.153 Hz at 25 A and 220 V (from Table 9). Table 10, the closest frequency to 0.153 Hz in Column 4, is 0.17 Hz. Therefore, f_2 (3.4 Hz, see Table 6) is selected for this design.

FREQUENCY OUTPUTS

Figure 2 shows a timing diagram for the various frequency outputs. The F1 and F2 outputs are the low frequency outputs that can be used to directly drive a stepper motor or electromechanical impulse counter. The F1 and F2 outputs provide two alternating low going pulses. The pulse width (t_1) is set at 275 ms, and the time between the falling edges of F1 and F2 (t_3) is approximately half the period of F1 (t_2). If, however, the period of F1 and F2 falls below 550 ms (1.81 Hz), the pulse width of F1 and F2 is set to half of their period. The maximum output frequencies for F1 and F2 are shown in Table 7.

The high frequency CF output is intended to be used for communications and calibration purposes. CF produces a 90 ms wide active high pulse (t_4) at a frequency proportional to active power. The CF output frequencies are listed in Table 8. As in the case of F1 and F2, if the period of CF (t_5) falls below 180 ms, the CF pulse width is set to half the period. For example, if the CF frequency is 20 Hz, the CF pulse width is 25 ms.

When the high frequency mode is selected (that is, SCF = 0, S1 = S0 = 1), the CF pulse width is fixed at 18 µs. Therefore, t_4 is always 18 µs, regardless of the output frequency on CF.

NO LOAD THRESHOLD

The ADE7755 also includes a no load threshold and start-up current feature that eliminates any creep effects in the meter. The ADE7755 is designed to issue a minimum output frequency in all modes except when SCF = 0 and S1 = S0 = 1. The no load detection threshold is disabled in this output mode to accommodate specialized application of the ADE7755. Any load generating a frequency lower than this minimum frequency will not cause a pulse to be issued on F1, F2, or CF. The minimum output frequency is given as 0.0014% of the full-scale output frequency for each of the f_i frequencies (i = 1, 2, 3, or 4), see Table 6.

For example, in an energy meter with a meter constant of 100 imp/kWh on F1 and F2 using f_2 (3.4 Hz), the maximum output frequency at F1 or F2 is 0.0014% of 3.4 Hz or 4.76×10^{-5} Hz. This is 3.05×10^{-3} Hz at CF (64 × F1 Hz). In this example, the no load threshold is equivalent to 1.7 W of the load or a start-up current of 8 mA at 220 V. IEC 1036 states that the meter must start up with a load current equal to or less than 0.4% Ib. For a 5 A (Ib) meter, 0.4% Ib is equivalent to 20 mA. The start-up current of this design therefore satisfies the IEC requirement. As illustrated in this example, the choice of f_i frequency (i = 1, 2, 3, or 4) and the ratio of the stepper motor display determine the start-up current.

OUTLINE DIMENSIONS

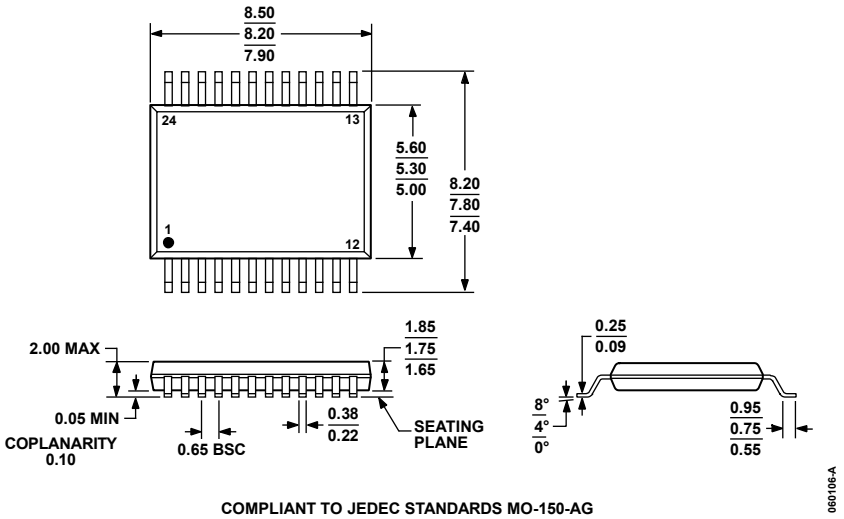


Figure 34. 24-Lead Shrink Small Outline Package [SSOP]
(RS-24)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADE7755ARSZ[1]	−40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP]	RS-24
ADE7755ARSRLZ[1]	−40°C to +85°C	24-Lead Shrink Small Outline Package [SSOP], 13″ Tape and Reel	RS-24
EVAL-ADE7755EBZ[1]	−40°C to +85°C	Evaluation Board	

[1] Z = RoHS Compliant Part.

ANALOG DEVICES

AN-559
APPLICATION NOTE

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106 • 781/329-4700 • World Wide Web Site: http://www.analog.com

A Low Cost Watt-Hour Energy Meter Based on the AD7755

By Anthony Collins

INTRODUCTION

This application note describes a low-cost, high-accuracy watt-hour meter based on the AD7755. The meter described is intended for use in single phase, two-wire distribution systems. However the design can easily be adapted to suit specific regional requirements, e.g., in the United States power is usually distributed to residential customers as single-phase, three-wire.

The AD7755 is a low-cost, single-chip solution for electrical energy measurement. The AD7755 is comprised of two ADCs, reference circuit, and all the signal processing necessary for the calculation of real (active) power. The AD7755 also includes direct drive capability for electromechanical counters (i.e., the energy register), and has a high-frequency pulse output for calibration and communications purposes.

This application note should be used in conjunction with the AD7755 data sheet. The data sheet provides detailed information on the functionality of the AD7755 and will be referenced several times in this application note.

DESIGN GOALS

The international Standard IEC1036 (1996-09) – *Alternating Current Watt-Hour Meters for Active Energy (Classes 1 and 2)*, was used as the primary specification for this design. For readers more familiar with the ANSI C12.16 specification, see the section at the end of this application note, which compares the IEC1036 and ANSI C12.16 standards. This section explains the key IEC1036 specifications in terms of their ANSI equivalents.

The design greatly exceeds this basic specification for many of the accuracy requirements, e.g., accuracy at unity-power factor and at low (PF = ±0.5) power factor. In addition, the dynamic range performance of the meter has been extended to 500. The IEC1036 standard specifies accuracy over a range of 5% Ib to I_{MAX}—see Table I. Typical values for I_{MAX} are 400% to 600% of Ib. Table I outlines the accuracy requirements for a static watt-hour meter. The current range (dynamic range) for accuracy is specified in terms of Ib (basic current).

Table I. Accuracy Requirements

Current Value[1]	PF[2]	Percentage Error Limits[3] Class 1	Class 2
0.05 Ib ≤ I < 0.1 Ib	1	±1.5%	±2.5%
0.1 Ib ≤ I ≤ I_{MAX}	1	±1.0%	±2.0%
0.1 Ib ≤ I ≤ 0.2 Ib	0.5 Lag	±1.5%	±2.5%
	0.8 Lead	±1.5%	
0.2 Ib ≤ I ≤ I_{MAX}	0.5 Lag	±1.0%	±2.0%
	0.8 Lead	±1.0%	

NOTES

[1]The current ranges for specified accuracy shown in Table I are expressed in terms of the basic current (Ib). The basic current is defined in IEC1036 (1996–09) section 3.5.1.1 as the value of current in accordance with which the relevant performance of a direct connection meter is fixed. I_{MAX} is the maximum current at which accuracy is maintained.

[2]Power Factor (PF) in Table I relates the phase relationship between the fundamental (45 Hz to 65 Hz) voltage and current waveforms. PF in this case can be simply defined as PF = cos(ϕ), where ϕ is the phase angle between pure sinusoidal current and voltage.

[3]Class index is defined in IEC1036 (1996–09) section 3.5.5 as the limits of the permissible percentage error. The percentage error is defined as:

$$Percentage\ Error = \frac{Energy\ Registered\ by\ Meter - True\ Energy}{True\ Energy} \times 100\%$$

The schematic in Figure 1 shows the implementation of a simple, low-cost watt-hour meter using the AD7755. A shunt is used to provide the current-to-voltage conversion needed by the AD7755 and a simple divider network attenuates the line voltage. The energy register (kWh) is a simple electromechanical counter that uses a two-phase stepper motor. The AD7755 provides direct drive capability for this type of counter. The AD7755 also provides a high-frequency output at the CF pin for the meter constant (3200 imp/kWh). Thus a high-frequency output is available at the LED and opto-isolator output. This high-frequency output is used to speed up the calibration process and provides a means of quickly verifying meter functionality and accuracy in a production environment. The meter is calibrated by varying the line voltage attenuation using the resistor network R5 to R14.

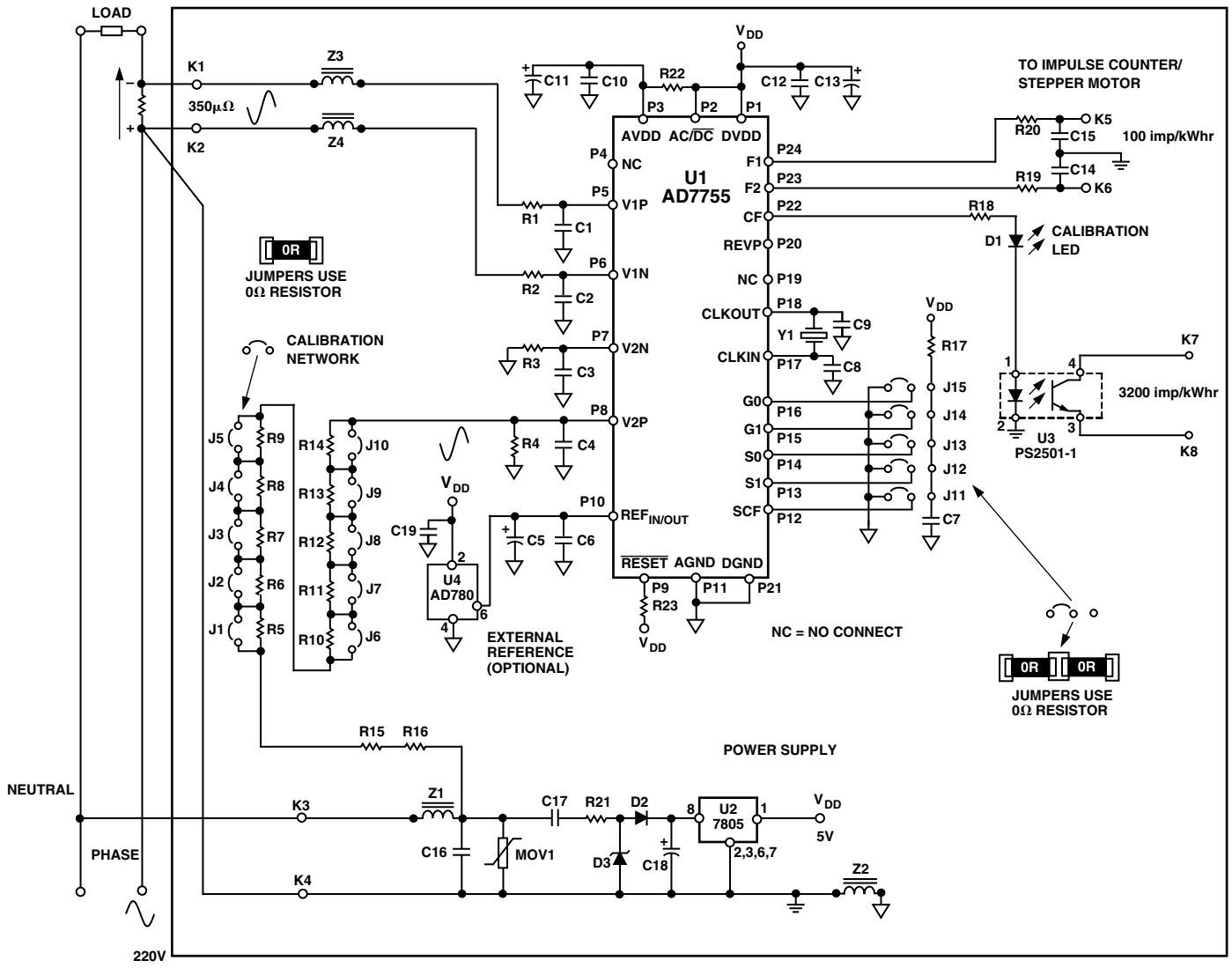


Figure 1. Simple Single-Phase Watt-Hour Meter Based on the AD7755

DESIGN EQUATIONS

The AD7755 produces an output frequency that is proportional to the time average value of the product of two voltage signals. The input voltage signals are applied at V1 and V2. The detailed functionality of the AD7755 is explained in the AD7755 data sheet, Theory Of Operation section. The AD7755 data sheet also provides an equation that relates the output frequency on F1 and F2 (counter drive) to the product of the rms signal levels at V1 and V2. This equation is shown here again for convenience and will be used to determine the correct signal scaling at V2 in order to calibrate the meter to a fixed constant.

$$Frequency = \frac{8.06 \times V1 \times V2 \times Gain \times F_{1-4}}{V_{REF}^{2}} \quad (1)$$

The meter shown in Figure 1 is designed to operate at a line voltage of 220 V and a maximum current (I_{MAX}) of 40 A. However, by correctly scaling the signals on Channel 1 and Channel 2, a meter operating of any line voltage and maximum current could be designed.

The four frequency options available on the AD7755 will allow similar meters (i.e., direct counter drive) with an I_{MAX} of up to 120 A to be designed. The basic current (Ib) for this meter is selected as 5 A and the current range for accuracy will be 2% Ib to I_{MAX}, or a dynamic range of 400 (100 mA to 40 A). The electromechanical register (kWh) will have a constant of 100 imp/kWh, i.e., 100 impulses from the AD7755 will be required in order to register 1 kWh. IEC1036 section 4.2.11 specifies that electromagnetic registers have their lowest values numbered in ten division, each division being subdivided into ten parts. Hence a display with a five plus one digits is used, i.e., 10,000s, 1,000s, 100s, 10s, 1s, 1/10s. The meter constant (for calibration and test) is selected as 3200 imp/kWh.

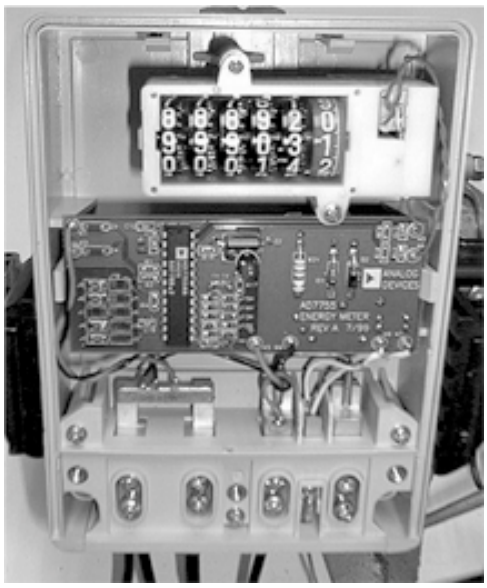


Figure 2. Final Implementation of the AD7755 Meter

AD7755 Reference

The schematic in Figure 1 also shows an optional reference circuit. The on-chip reference circuit of the AD7755 has a temperature coefficient of typically 30 ppm/°C. However, on A Grade parts this specification is not guaranteed and may be as high as 80 ppm/°C. At 80 ppm/°C the AD7755 error at –20°C/+60°C could be as high as 0.65%, assuming a calibration at 25°C.

Shunt Selection

The shunt size (350 μΩ) is selected to maximize the use of the dynamic range on Channel V1 (current channel). However there are some important considerations when selecting a shunt for an energy metering application. First, minimize the power dissipation in the shunt. The maximum rated current for this design is 40 A, therefore, the maximum power dissipated in the shunt is $(40\ A)^2 \times 350\ \mu\Omega = 560$ mW. IEC1036 calls for a maximum power dissipation of 2 W (including power supply). Secondly, the higher power dissipation may make it difficult to manage the thermal issues. Although the shunt is manufactured from Manganin material, which is an alloy with a low temperature coefficient of resistance, high temperatures may cause significant error at heavy loads. A third consideration is the ability of the meter to resist attempts to tamper by shorting the phase circuit. With a very low value of shunt resistance the effects of externally shorting the shunt are very much minimized. Therefore, the shunt should always be made as small as possible, but this must be offset against the signal range on V1 (0 mV–20 mV rms with a gain of 16). If the shunt is made too small it will not be possible to meet the IEC1036 accuracy requirements at light loads. A shunt value of 350 μΩ was considered a good compromise for this design.

Design Calculations

Design parameters:

Line voltage = 220 V (nominal)
I_{MAX} = 40 A (Ib = 5 A)
Counter = 100 imp/kWh
Meter constant = 3200 imp/kWh
Shunt size = 350 μΩ
100 imp/hour = 100/3600 sec = 0.027777 Hz
Meter will be calibrated at Ib (5A)
Power dissipation at Ib = 220 V × 5 A = 1.1 kW
Frequency on F1 (and F2) at Ib = 1.1 × 0.027777 Hz
= 0.0305555 Hz

Voltage across shunt (V1) at Ib = 5 A × 350 μΩ = 1.75 mV.

To select the F_{1-4} frequency for Equation 1 see the AD7755 data sheet, Selecting a Frequency for an Energy Meter Application section. From Tables V and VI in the AD7755 data sheet it can be seen that the best choice of frequency for a meter with I_{MAX} = 40 A is 3.4 Hz (F_2). This frequency selection is made by the logic inputs S0 and S1—see Table II in the AD7755 data sheet. The CF frequency selection (meter constant) is selected by using the logic input SCF. The two available options are 64 × F1(6400 imp/kWh) or 32 × F1(3200 imp/kWh). For this design, 3200 imp/kWh is selected by setting SCF logic low. With a meter constant of 3200 imp/kWh and a maximum current of 40 A, the maximum frequency from CF is 7.82 Hz. Many calibration benches used to verify meter accuracy still use optical techniques. This limits the maximum frequency that can be reliably read to about 10 Hz. The only remaining unknown from equation 1 is V2 or the signal level on Channel 2 (the voltage channel).

From Equation 1 on the previous page:

$$0.030555\ Hz = \frac{8.06 \times 1.75\ mV \times V2 \times 16 \times 3.4\ Hz}{2.5^2}$$

V2 = 248.9 mV rms

Therefore, in order to calibrate the meter the line voltage needs to be attenuated down to 248.9 mV.

CALIBRATING THE METER

From the previous section it can be seen that the meter is simply calibrated by attenuating the line voltage down to 248.9 mV. The line voltage attenuation is carried out by a simple resistor divider as shown in Figure 3. The attenuation network should allow a calibration range of at least ±30% to allow for shunt tolerances and the on-chip reference tolerance of ±8%—see AD7755 data sheet. In addition, the topology of the network is such that the phase-matching between Channel 1 and Channel 2 is preserved, even when the attenuation is being adjusted (see Correct Phase Matching Between Channels section).

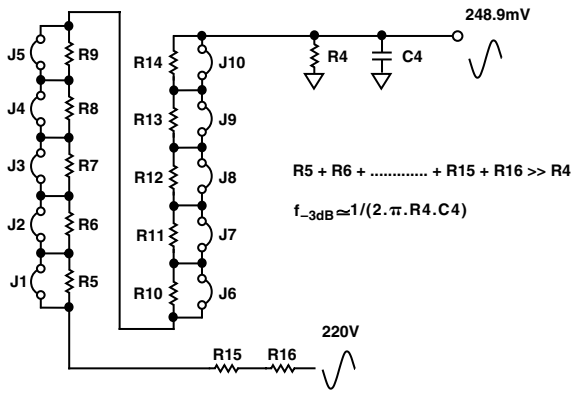


Figure 3. Attenuation Network

As can be seen from Figure 3, the –3 dB frequency of this network is determined by R4 and C4. Even with all the jumpers closed, the resistance of R15 (330 kΩ) and R16 (330 kΩ) is still much greater than R4 (1 kΩ). Hence varying the resistance of the resistor chain R5 to R14 will have little effect on the –3 dB frequency of the network. The network shown in Figure 3 allows the line voltage to be attenuated and adjusted in the range 175 mV to 333 mV with a resolution of 10 bits or 154 μV. This is achieved by using the binary weighted resistor chain R5 to R14. This will allow the meter to be accurately calibrated using a successive approximation technique. Starting with J1, each jumper is closed in order of ascendance, e.g., J1, J2, J3, etc. If the calibration frequency on CF, i.e., 32 × 100 imp/hr (0.9777 Hz), is exceeded when any jumper is closed, it should be opened again. All jumpers are tested, J10 being the last jumper. Note jumper connections are made with 0 Ω fixed resistors which are soldered into place. This approach is preferred over the use of trim pots, as the stability of the latter over time and environmental conditions is questionable.

Since the AD7755 transfer function is extremely linear a one-point calibration (Ib) at unity power factor, is all that is needed to calibrate the meter. If the correct precautions have been taken at the design stage, no calibration will be necessary at low-power factor (PF = 0.5). The next section discusses phase matching for correct calculation of energy at low-power factor.

CORRECT PHASE MATCHING BETWEEN CHANNELS

The AD7755 is internally phase-matched over the frequency range 40 Hz to 1 kHz. Correct phase matching is important in an energy metering application because any phase mismatch between channels will translate into significant measurement error at low-power factor. This is easily illustrated with the following example. Figure 4 shows the voltage and current waveforms for an inductive load. In the example shown, the current lags the voltage by 60° (PF = –0.5). Assuming pure sinusoidal conditions, the power is easily calculated as V rms × I rms × cos (60°).

If, however, a phase error (ϕ_e) is introduced externally to the AD7755, e.g., in the antialias filters, the error is calculated as:

$$[\cos(\delta^\circ) - \cos(\delta^\circ + \phi_e)]/\cos(\delta^\circ) \times 100\% \quad (2)$$

See Note 3 on Table I. Where δ is the phase angle between voltage and current and ϕ_e is the external phase error. With a phase error of 0.2°, for example, the error at PF = 0.5 (60°) is calculated as 0.6%. As this example demonstrates, even a very small phase error will produce a large measurement error at low power factor.

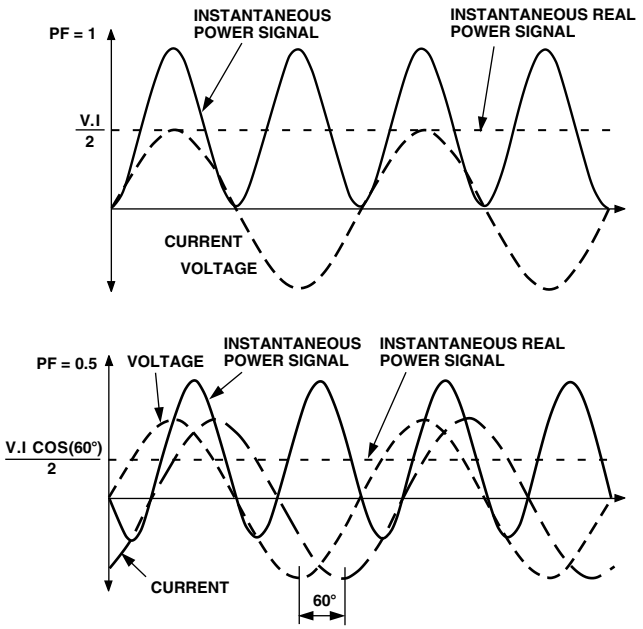


Figure 4. Voltage and Current (Inductive Load)

ANTIALIAS FILTERS

As mentioned in the previous section, one possible source of external phase errors are the antialias filters on Channel 1 and Channel 2. The antialias filters are low-pass filters that are placed before the analog inputs of any ADC. They are required to prevent a possible distortion due to sampling called aliasing. Figure 5 illustrates the effects of aliasing.

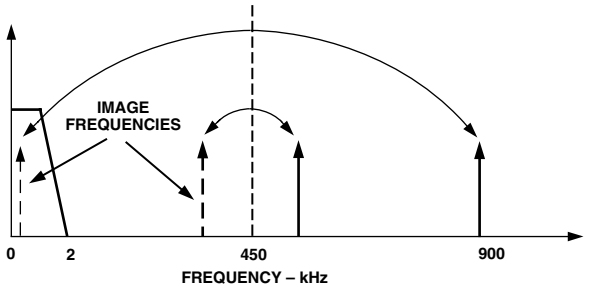


Figure 5. Aliasing Effects

Figure 5 shows how aliasing effects could introduce inaccuracies in an AD7755-based meter design. The AD7755 uses two Σ-Δ ADCs to digitize the voltage and current signals. These ADCs have a very high sampling rate, i.e., 900 kHz. Figure 5 shows how frequency components (arrows shown in black) above half the sampling frequency (also know as the Nyquist frequency), i.e., 450 kHz is imaged or folded back down below 450 kHz (arrows shown dashed). This will happen with all ADCs no matter what the architecture. In the example shown it can be seen that only frequencies near the sampling frequency, i.e., 900 kHz, will move into the band of interest for metering, i.e., 0 kHz–2 kHz. This fact will allow us to use a very simple LPF (Low-Pass Filter) to attenuate these high frequencies (near 900 kHz) and so prevent distortion in the band of interest.

The simplest form of LPF is the simple RC filter. This is a single-pole filter with a roll-off or attenuation of –20 dBs/dec.

Choosing the Filter –3 dB Frequency

As well as having a magnitude response, all filters also have a phase response. The magnitude and phase response of a simple RC filter (R = 1 kΩ, C = 33 nF) are shown in Figures 6 and 7. From Figure 6 it is seen that the attenuation at 900 kHz for this simple LPF is greater than 40 dBs. This is enough attenuation to ensure no ill effects due to aliasing.

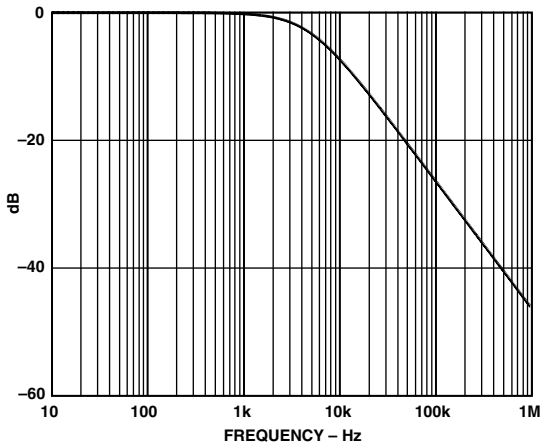


Figure 6. RC Filter Magnitude Response

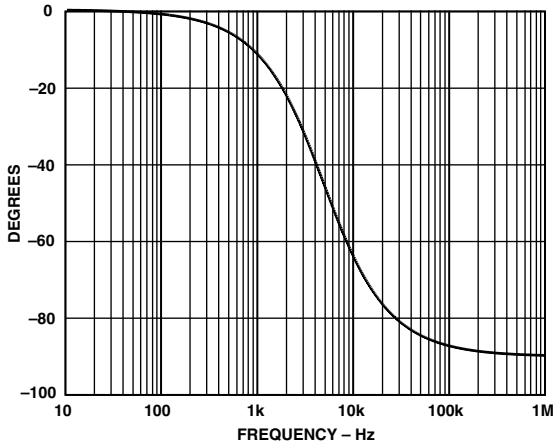


Figure 7. RC Filter Phase Response

As explained in the last section, the phase response can introduce significant errors if the phase response of the LPFs on both Channel 1 and Channel 2 are not matched. Phase mismatch can easily occur due to poor component tolerances in the LPF. The lower the –3 dB frequency in the LPF (antialias filter) the more pronounced these errors will be at the fundamental frequency component or the line frequency. Even with the corner frequency set at 4.8 kHz (R = 1 kΩ, C = 33 nF) the phase errors due to poor component tolerances can be significant. Figure 8 illustrates the point. In Figure 8, the phase response for the simple LPF is shown at 50 Hz for R = 1 kΩ ± 10%, C = 33 nF ± 10%. Remember a phase shift of 0.2° can causes measurement errors of 0.6% at low-power factor. This design uses resistors of 1% tolerance and capacitors of 10% tolerance for the antialias filters to reduce the possible problems due to phase mismatch. Alternatively the corner frequency of the antialias filter could be pushed out to 10 kHz–15 Hz. However, the corner frequency should not be made too high, as this could allow enough high-frequency components to be aliased and so cause accuracy problems in a noisy environment.

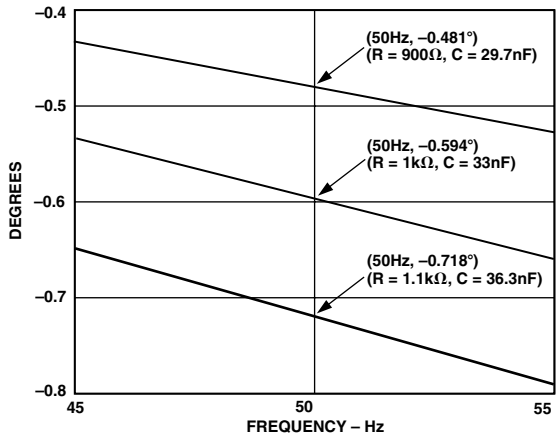


Figure 8. Phase Shift at 50 Hz Due to Component Tolerances

Note that this is also why precautions were taken with the design of the calibration network on Channel 2 (voltage channel). Calibrating the meter by varying the resistance of the attenuation network will not vary the –3 dB frequency and hence the phase response of the network on Channel 2—see Calibrating the Meter section. Shown in Figure 9 is a plot of phase lag at 50 Hz when the resistance of the calibration network is varied from 660 kΩ (J1–J10 closed) to 1.26 MΩ (J1–J10 open).

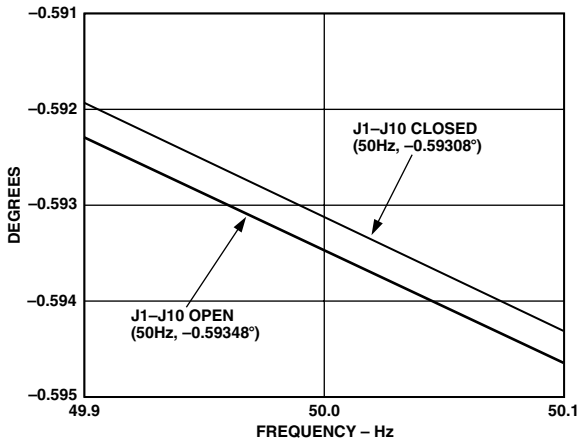


Figure 9. Phase Shift Due to Calibration

COMPENSATING FOR PARASITIC SHUNT INDUCTANCE

When used at low frequencies a shunt can be considered a purely resistive element with no significant reactive elements. However, under certain situations even a small amount of stray inductance can cause undesirable effects when a shunt is used in a practical data acquisition system. The problem is very noticeable when the resistance of the shunt is very low, in the order of 200 μΩ. Shown below is an equivalent circuit for the shunt used in the AD7755 reference design. There are three connections to the shunt. One pair of connections provides the current sense inputs (V1P and V1N) and the third connection is the ground reference for the system.

The shunt resistance is shown as R_{SH1} (350 μΩ). R_{SH2} is the resistance between the V1N input terminal and the system ground reference point. The main parasitic elements (inductance) are shown as L_{SH1} and L_{SH2}. Figure 10 also shows how the shunt is connected to the AD7755 inputs (V1P and V1N) through the antialias filters. The function of the antialias filters is explained in the previous section and their ideal magnitude and phase responses are shown in Figures 6 and 7.

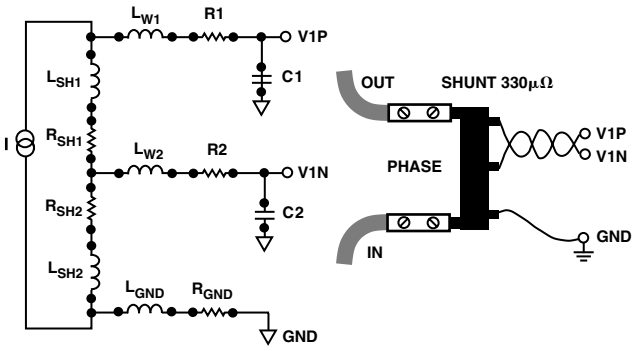


Figure 10. Equivalent Circuit for the Shunt

Canceling the Effects of the Parasitic Shunt Inductance

The effect of the parasitic shunt inductance is shown in Figure 11. The plot shows the phase and magnitude response of the antialias filter network with and without (dashed) a parasitic inductance of 2 nH. As can be seen from the plot, both the gain and phase response of the network are affected. The attenuation at 1 MHz is now only about –15 dB, which could cause some repeatability and accuracy problems in a noisy environment. More importantly, a phase mismatch may now exist between the current and voltage channels. Assuming the network on Channel 2 has been designed to match the ideal phase response of Channel 1, there now exists a phase mismatch of 0.1° at 50 Hz. Note that 0.1° will cause a 0.3% measurement error at PF = ±0.5. See Equation 2 (Correct Phase Matching Between Channels).

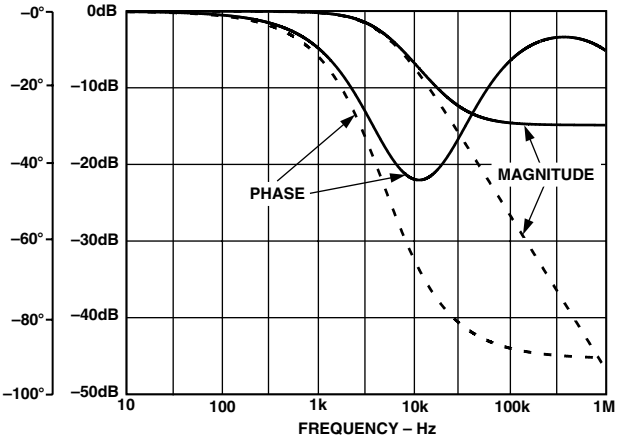


Figure 11. Effect of Parasitic Shunt Inductance on the Antialias Network

The problem is caused by the addition of a zero into the antialias network. Using the simple model for the shunt shown in Figure 10, the location of the zero is given as R_{SH1}/L_{SH1} radians.

One way to cancel the effects of this additional zero in the network is to add an additional pole at (or close to) the same location. The addition of an extra RC on each analog input of Channel 1 will achieve the additional

pole required. The new antialias network for Channel 1 is shown in Figure 12. To simplify the calculation and demonstrate the principle, the Rs and Cs of the network are assumed to have the same value.

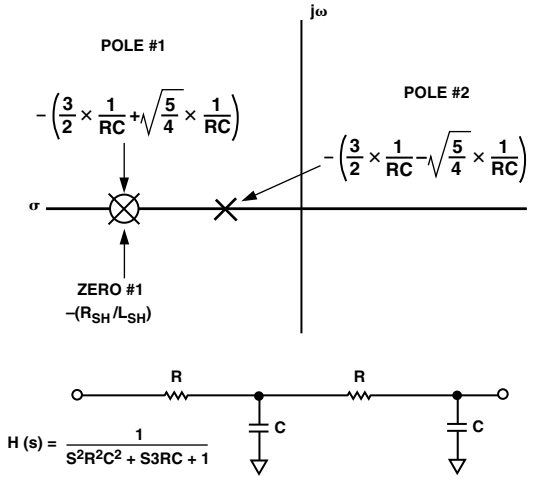


Figure 12. Shunt Inductance Compensation Network

Figure 12 also gives an expression for the location of the poles of this compensation network. The purpose of Pole #1 is to cancel the effects of the zero due to the shunt inductance. Pole #2 will perform the function of the antialias filters as described in the Antialias Filters section. The following illustrates a sample calculation for a shunt of 330 μΩ with a parasitic inductance of 2 nH.

The location of the pole #1 is given as:

$$-\left(\frac{3}{2}\times\frac{1}{RC}+\sqrt{\frac{5}{4}}\times\frac{1}{\mathrm{RC}}\right)=\frac{R_{SH1}}{L_{SH1}}$$

For R_{SH1} = 330 μΩ, L_{SH1} = 2 nH, C = 33 nF

R is calculated as approximately 480 Ω (use 470 Ω).

The location of Pole #1 is 165,000 rads or 26.26 kHz.

This places the location of Pole # 2 at:

$$-\left(\frac{3}{2}\times\frac{1}{\mathrm{RC}}+\sqrt{\frac{5}{4}}\times\frac{1}{\mathrm{RC}}\right)=3.838\ kHz$$

To ensure phase-matching between Channel 1 and Channel 2, the pole at Channel 2 must also be positioned at this location. With C = 33 nF, the new value of resistance for the antialias filters on Channel 2 is approximately 1.23 kΩ (use 1.2 kΩ).

Figure 13 shows the effect of the compensation network on the phase and magnitude response of the antialias network in Channel 1. The dashed line shows the response of Channel 2 using practical values for the newly calculated component values, i.e., 1.2 kΩ and 33 nF. The solid line shows the response of Channel 1 with the parasitic shunt inductance included. Notice phase and magnitude responses match very closely with the ideal response—shown as a dashed line. This is the objective of the compensation network.

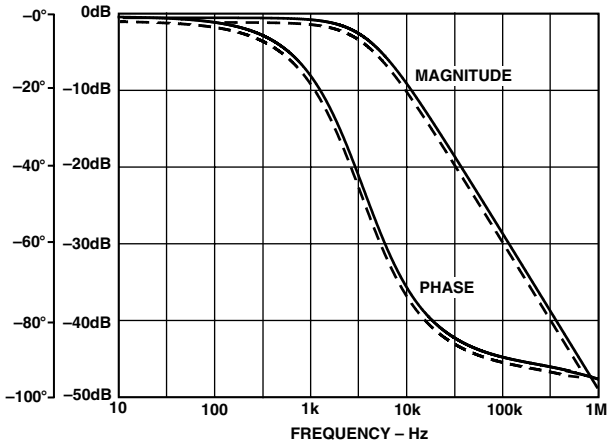


Figure 13. Antialias Network Phase and Magnitude Response after Compensation

The method of compensation works well when the pole due to shunt inductance is less than 25 kHz or so. If zero is at a much higher frequency its effects may simply be eliminated by placing an extra RC on Channel 1 with a pole that is a decade greater than that of the antialias filter, e.g., 100 Ω and 33 nF.

Care should be taken when selecting a shunt to ensure its parasitic inductance is small. This is especially true of shunts with small values of resistance, e.g., <200 μΩ. Note that the smaller the shunt resistance, the lower the zero frequency for a given parasitic inductance (Zero = R_{SH1}/L_{SH1}).

POWER SUPPLY DESIGN

This design uses a simple low-cost power supply based on a capacitor divider network, i.e., C17 and C18. Most of the line voltage is dropped across C17, a 470 nF 250 V metalized polyester film capacitor. The impedance of C17 dictates the effective VA rating of the supply. However the size of C17 is constrained by the power consumption specification in IEC1036. The total power consumption in the voltage circuit, including power supply, is specified in section 4.4.1.1 of IEC1036 (1996-9). The total power consumption in each phase is 2 W and 10 VA under nominal conditions. The nominal VA rating of the supply in this design is 7 VA. The total power dissipation is approximately 0.5 W. Together with the power dissipated in the shunt at 40 A load, the total power consumption of the meter is 1.06 W. Figure 14 shows the basic power supply design.

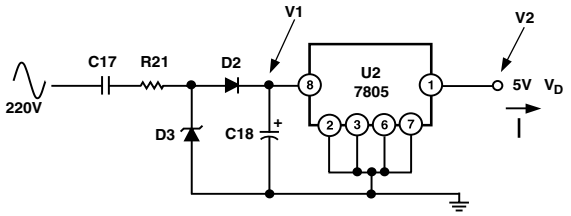


Figure 14. Power Supply

The plots shown in Figures 15, 16, 17, and 18 show the PSU performance under heavy load (50 A) with the line voltage varied from 180 V to 250 V. By far the biggest load on the power supply is the current required to drive the stepper motor which has a coil impedance of about 400 Ω. This is clearly seen by looking at V1 (voltage on C18) in the plots below. Figure 16 shows the current drawn from the supply. Refer to Figure 14 when reviewing the simulation plots below.

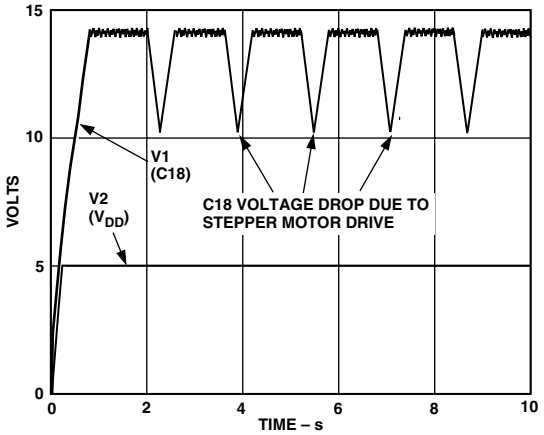


Figure 15. Power Supply Voltage Output at 220 V and 50 A Load

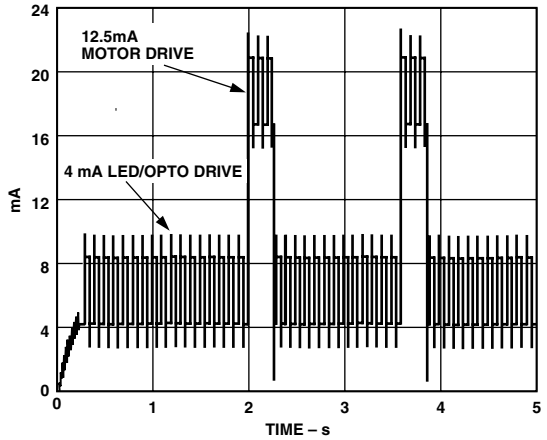


Figure 16. Power Supply Current Output at 220 V and 50 A Load

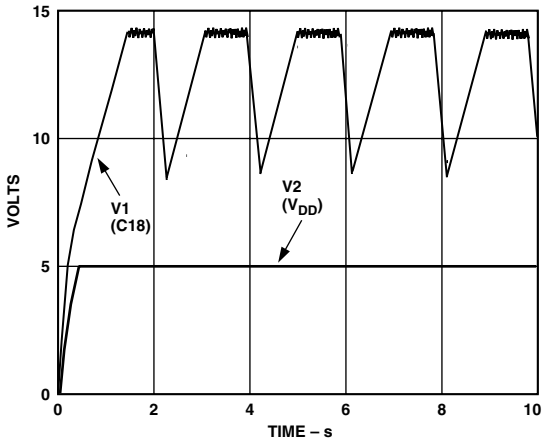


Figure 17. Power Supply Voltage Output at 180 V and 50 A Load

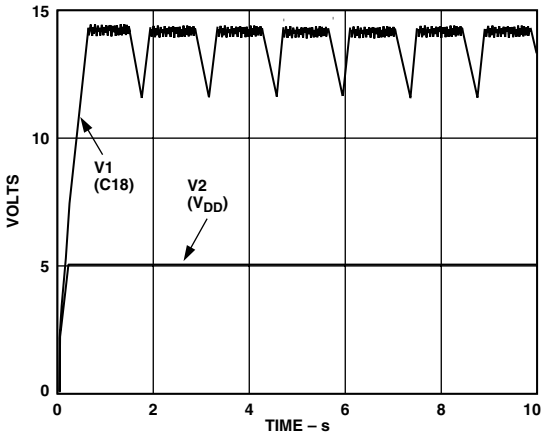


Figure 18. Power Supply Voltage Output at 250 V and 50 A Load

DESIGN FOR IMMUNITY TO ELECTROMAGNETIC DISTURBANCE

In Section 4.5 of IEC1036 it is stated that "the meter shall be designed in such a way that conducted or radiated electromagnetic disturbances as well as electrostatic discharge do not damage nor substantially influence the meter." The considered disturbances are:

1. Electrostatic Discharge
2. Electromagnetic HF Fields
3. Fast Transience Burst

All of the precautions and design techniques (e.g., ferrite beads, capacitor line filters, physically large SMD resistors, PCB layout including grounding) contribute to a certain extent in protecting the meter electronics from each form of electromagnetic disturbance. Some precautions (e.g., ferrite beads), however, play a more important role in the presence of certain kinds of disturbances (e.g., RF and fast transience burst). The following discuses each of the disturbances listed above and details what protection has been put in place.

ELECTROSTATIC DISCHARGE (ESD)

Although many sensitive electronic components contain a certain amount of ESD protection on-chip, it is not possible to protect against the kind of severe discharge described below. Another problem is that the effect of an ESD discharge is cumulative, i.e., a device may survive an ESD discharge, but it is no guarantee that it will survive multiple discharges at some stage in the future. The best approach is to eliminate or attenuate the effects of the ESD event before it comes in contact with sensitive electronic devices. This holds true for all conducted electromagnetic disturbances. This test is carried out according to IEC1000-4-2, under the following conditions:

– Contact Discharge;
– Test Severity Level 4;
– Test Voltage 8 kV;
– 10 Discharges.

Very often no additional components are necessary to protect devices. With a little care those components already required in the circuit can perform a dual role. For example, the meter must be protected from ESD events at those points where it comes in contact with the "outside world," e.g., the connection to the shunt. Here the AD7755 is connected to the shunt via two LPFs (antialias filters) which are required by the ADC—see Antialias Filters section. This RC filter can also be enough to protect against ESD damage to CMOS devices. However, some care must be taken with the type of components used. For example, the resistors should not be wire-wound as the discharge will simply travel across them. The resistors should also be physically large to stop the discharge arcing across the resistor. In this design 1/8W SMD 1206 resistors were used in the antialias filters. Two ferrite beads are also placed in series with the connection to the shunt. A ferrite choke is particularly effective at slowing the fast rise time of an ESD current pulse. The high-frequency transient energy is absorbed in the ferrite material rather than being diverted or reflected to another part of the system. (*The properties of ferrite are discussed later.*) The PSU circuit is also directly connected to the terminals of the meter. Here the discharge will be dissipated by the ferrite, the line filter capacitor (C16), and the rectification diodes D2 and D3. The analog input V2P is protected by the large impedance of the attenuation network used for calibration.

Another very common low-cost technique employed to arrest ESD events is to use a spark gap on the component side of the PCB—see Figure 19. However, since the meter will likely operate in an open air environment and be subject to many discharges, this is not recommended at sensitive nodes like the shunt connection. Multiple discharges could cause carbon buildup across the spark gap which could cause a short or introduce an impedance that will in time affect accuracy. A spark gap was introduced in the PSU after the MOV to take care of any very high amplitude/fast rise time discharges.

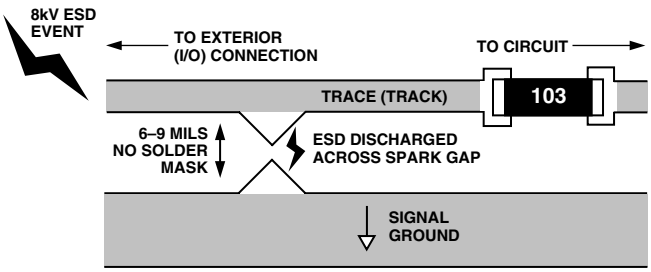


Figure 19. Spark Gap to Arrest ESD Events

ELECTROMAGNETIC HF FIELDS

Testing is carried out according to IEC100-4-3. Susceptibility of integrated circuits to RF tends to be more pronounced in the 20 MHz–200 MHz region. Frequencies higher that this tend to be shunted away from sensitive devices by parasitic capacitances. In general, at the IC level, the effects of RF in the region 20 MHz–200 MHz will tend to be broadband in nature, i.e., no individual frequency is more troublesome than another. However, there may be higher sensitivity to certain frequencies due to resonances on the PCB. These resonances could cause insertion gain at certain frequencies which, in turn, could cause problems for sensitive devices. By far the greatest RF signal levels are those coupled into the system via cabling. These connection points should be protected. Some techniques for protecting the system are:

1. Minimize Circuit Bandwidth
2. Isolate Sensitive Parts of the System

Minimize Bandwidth

In this application the required analog bandwidth is only 2 kHz. This is a significant advantage when trying to reduce the effects of RF. The cable entry points can be low-pass filtered to reduce the amount of RF radiation entering the system. The shunt output is already filtered before being connected to the AD7755. This is to prevent aliasing effects that were described earlier. By choosing the correct components and adding some additional components (e.g., ferrite beads) these antialias filters can double as very effective RF filters. Figure 7 shows a somewhat idealized frequency response for the antialias filters on the analog inputs. When considering higher frequencies (e.g., > 1 MHz), the parasitic reactive elements of each lumped component must be considered. Figure 20 shows the antialias filters with the parasitic elements included. These small values of parasitic capacitance and inductance become significant at higher frequencies and therefore must be considered.

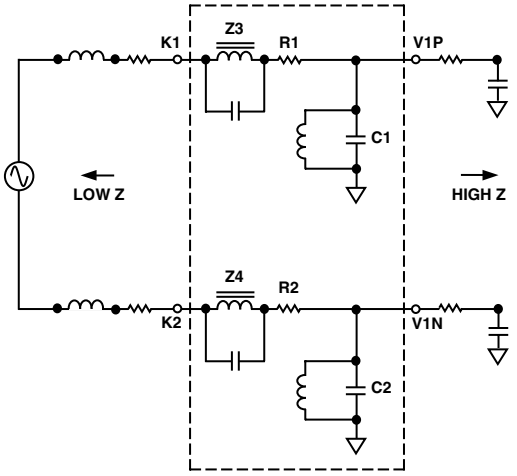


Figure 20. Antialias Filters Showing Parasitics

Parasitics can be kept at a minimum by using physically small components with short lead lengths (i.e., surface mount). Because the exact source impedance conditions are not known (this will depend on the source impedance of the electricity supply), some general precautions should be taken to minimize the effects of potential resonances. Resonances that result from the interaction of the source impedance and filter networks could cause insertion gain effects and so increase the exposure of the system to RF radiation at certain (resonant) frequencies. Lossy (i.e., having large resistive elements) components like capacitors with lossy dielectric (e.g., Type X7R) and ferrite are ideal components for reducing the "Q" of the input network. The RF radiation is dissipated as heat, rather than being reflected or diverted to another part of the system. The ferrite beads Z3 and Z4 perform very well in this respect. Figure 21 shows how the impedance of the ferrite beads varies with frequency.

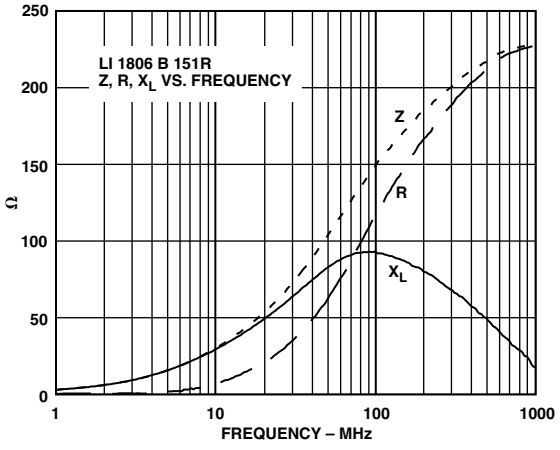


Figure 21. Frequency Response of the Ferrite Chips (Z3 and Z4) in the Antialias Filter

From Figure 21 it can be seen that the ferrite material becomes predominately resistive at high frequencies. Note also that the impedance of the ferrite material increases with frequency, causing only high (RF) frequencies to be attenuated.

Isolation

The shunt connection is the only location where the AD7755 is connected directly (via antialias filters) to the "outside world." The system is also connected to the phase and neutral lines for the purpose of generating a power supply and voltage channel signal (V2). The ferrite bead (Z1) and line filter capacitor (C16) should significantly reduce any RF radiation on the power supply.

Another possible path for RF is the signal ground for the system. A moating technique has been used to help isolate the signal ground surrounding the AD7755 from the external ground reference point (K4). Figure 22 illustrates the principle of this technique called partitioning or "moating."

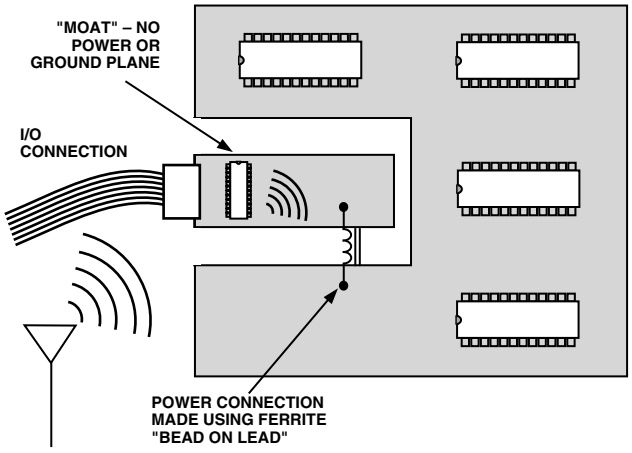


Figure 22. High-Frequency Isolation of I/O Connections Using a "Moat"

Sensitive regions of the system are protected from RF radiation entering the system at the I/O connection. An area surrounding the I/O connection does not have any ground or power planes. This limits the conduction paths for RF radiation and is called a "moat." Obviously power, ground, and signal connections must cross this moat and Figure 22 shows how this can be safely achieved by using a ferrite bead. Remember that ferrite offers a large impedance to high frequencies (see Figure 21).

ELECTRICAL FAST TRANSIENCE (EFT) BURST TESTING

This testing determines the immunity of a system to conducted transients. Testing is carried out in accordance with IEC1000-4-4 under well-defined conditions. The EFT pulse can be particularly difficult to guard against because the disturbance is conducted into the system via external connections, e.g., power lines. Figure 23 shows the physical properties of the EFT pulse used in IEC1000-4-4. Perhaps the most debilitating attribute of the pulse is not its amplitude (which can be as high as 4 kV), but

the high-frequency content due to the fast rise times involved. Fast rise times mean high-frequency content which allows the pulse to couple to other parts of the system through stray capacitance, etc. Large differential signals can be generated by the inductance of PCB traces and signal ground. These large differential signals could interrupt the operation of sensitive electronic components. Digital systems are generally most at risk because of data corruption. Analog electronic systems tend only to be affected for the duration of the disturbance.

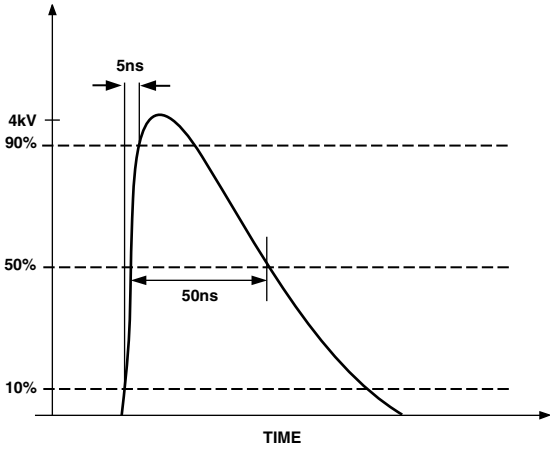


Figure 23. Single EFT Pulse Characteristics

Another possible issue with conducted EFT is that the effects of the radiation will, like ESD, generally be cumulative for electronic components. The energy in an EFT pulse can be as high as 4 mJ and deliver 40 A into a 50 Ω load (see Figure 26). Therefore continued exposure to EFT due to inductive load switching etc., may have implications for the long-term reliability of components. The best approach is to protect those parts of the system that could be sensitive to EFT.

The protection techniques described in the last section (Electromagnetic HF Fields) also apply equally well in the case of EFT. The electronics should be isolated as much as possible from the source of the disturbance through PCB layout (i.e., moating) and filtering signal and power connections. In addition, a 10 nF capacitor (C16) placed across the mains provides a low impedance shunt for differential EFT pulses. Stray inductance due to leads and PCB traces will mean that the MOV will not be very effective in attenuating the differential EFT pulse. The MOV is very effective in attenuating high energy, relatively long duration disturbances, e.g., due to lighting strikes, etc. The MOV is discussed in the next section.

MOV Type S20K275

The MOV used in this design was of type S20K275 from Siemens. An MOV is basically a voltage-dependant resistor whose resistance decreases with increasing voltage. They are typically connected in parallel with the device or circuit being protected. During an overvoltage event they form a low-resistance shunt and thus prevent any further rise in the voltage across the circuit being protected. The overvoltage is essentially dropped across the source impedance of the overvoltage source, e.g., the mains network source impedance. Figure 24 illustrates the principle of operation.

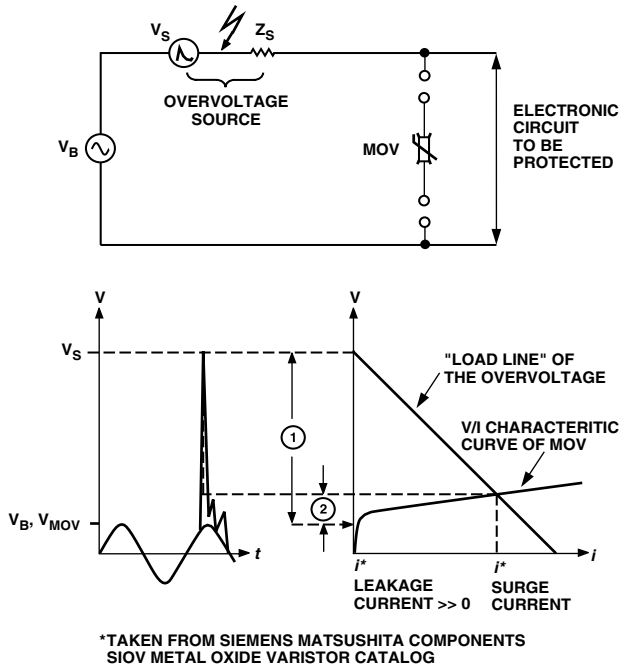


Figure 24. Principle of MOV Overvoltage Protection

The plot in Figure 24 shows how the MOV voltage and current can be estimated for a given overvoltage and source impedance. A load line (open-circuit voltage, short-circuit current) is plotted on the same graph as the MOV characteristic curve. Where the curves intersect, the MOV clamping voltage and current can be read. Note that care must be taken when determining the short-circuit current. The frequency content of the overvoltage must be taken into account as the source impedance (e.g., mains) may vary considerably with frequency. A typical impedance of 50 Ω is used for mains source impedance during fast transience (high-frequency) pulse testing. The next section discusses IEC1000-4-4 and IEC1000-4-5, which are transience and overvoltage EMC compliance tests.

IEC1000-4-4 and the S20K275

While the graphical technique just described is useful, an even better approach is to use simulation to obtain a better understanding of MOV operation. EPCOS Components provides SPICE models for all their MOVs and these are very useful in determining device operation under the various IEC EMC compliance tests. For more information on EPCOS SPICE models and their applications see:

http://www.epcos.de/inf/70/e0000000.htm

The purpose of IEC1000-4-4 is to determine the effect of repetitive, low energy, high-voltage, fast rise time pulses on an electronic system. This test is intended to simulate transient disturbances such as those originating from switching transience (e.g., interruption of inductive loads, relay contact bounce, etc.).

Figure 25 shows an equivalent circuit intended to replicate the EFT test pulse as specified in IEC1000-4-4. The generator circuit is based on Figure 1 IEC1000-4-4 (1995-01). The characteristics of operation are:

– Maximum energy of 4 mJ/pulse at 2 kV into 50 Ω
– Source impedance of 50 Ω ± 20%
– DC blocking capacitor of 10 nF
– Pulse rise time of 5 ns ± 30%
– Pulse duration (50% value) of 50 ns ± 30%
– Pulse shape as shown in Figure 23.

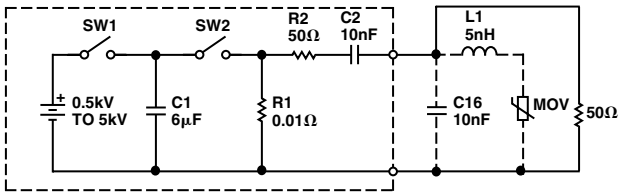


Figure 25. EFT Generator

The simulated output of this generator delivered to a purely resistive 50 Ω load is shown in Figure 26. The open-circuit output pulse amplitude from the generator is 4 kV. Therefore, the source impedance of the generator is 50 Ω as specified by the IEC1000-4-4, i.e., ratio of peak pulse output unloaded and loaded (50 Ω) is 2:1.

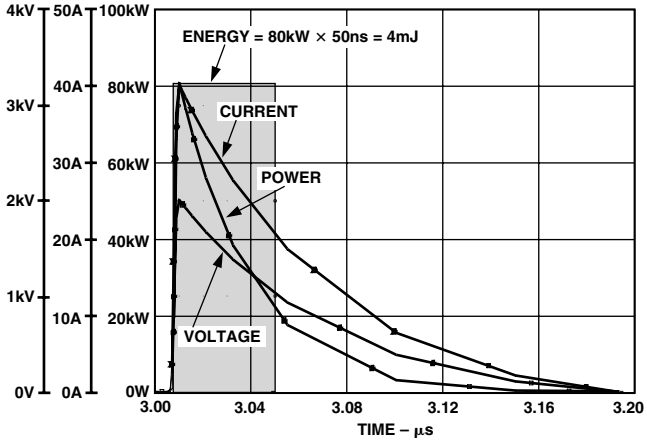


Figure 26. EFT Generator Output into 50 Ω (No Protection)

The plot in Figure 26 also shows the current and instantaneous power (V × I) delivered to the load. The total energy is the integral of the power and can be approximated by the rectangle method as shown. It is approximately 4 mJ at 2 kV as per specification.

Figure 27 shows the generator output into 50 Ω load with the MOV and some inductance (5 nH). This is included to take into account stray inductance due to PCB traces and leads. Although the simulation result shows that the EFT pulse has been attenuated (600 V) and most of the energy being absorbed by the MOV (only 0.8 mJ is delivered to the 50 Ω load) it should be noted that stray inductance and capacitance could render the MOV unless. For example Figure 28 shows the same simulation with the stay inductance increased to 1 μH, which could easily happen if proper care is not taken with the layout. The pulse amplitude reaches 2 kV once again.

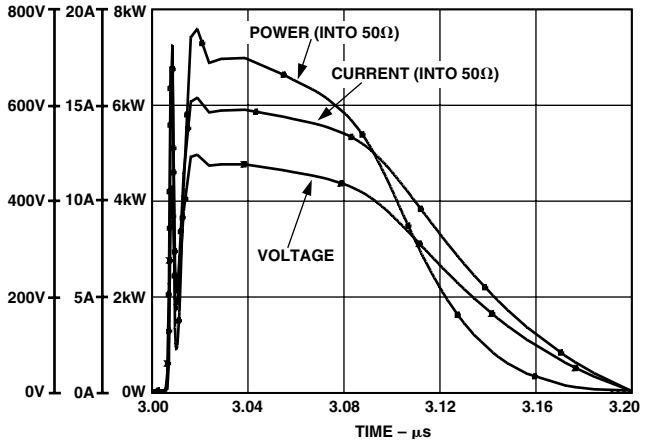


Figure 27. EFT Generator Output into 50 Ω with MOV in Place

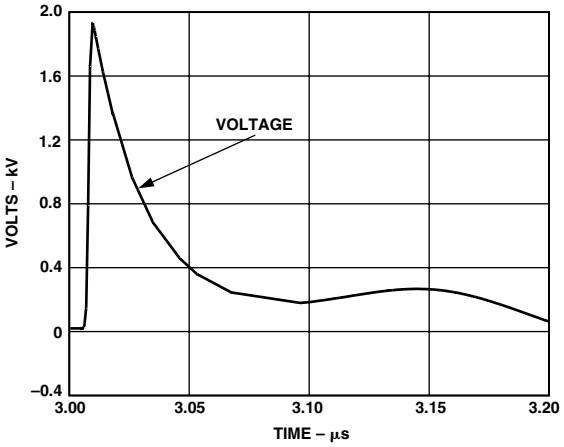


Figure 28. EFT Generator Output into 50 Ω with MOV in Place and Stray Inductance of 1 μH

When the 10 nF Capacitor (C16) is connected, a low impedance path is provided for differential EFT pulses. Figure 29 shows the effect of connecting C16. Here the stray inductance (L1) is left at 1 μH and the MOV is in place. The plot shows the current through C16 and the voltage across the 50 Ω load. The capacitor C16 provides a low impedance path for the EFT pulse. Note the peak current through C16 of 80 A. The result is that the amplitude of the EFT pulse is greatly attenuated.

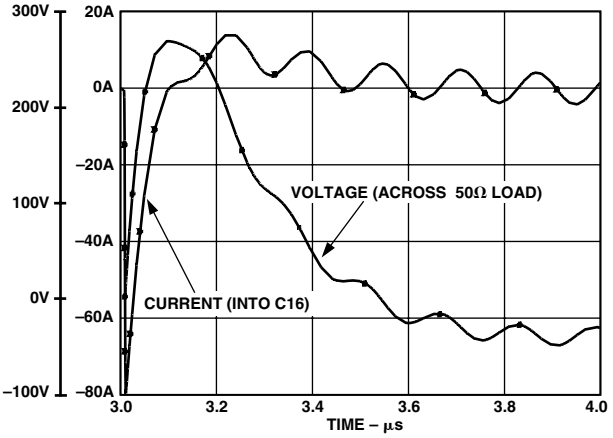


Figure 29. EFT Generator Output into 50 Ω with MOV in Place, Stray Inductance of 1 μH and C16 (10 nF) in Place

IEC1000-4-5

The purpose of IEC1000-4-5 is to establish a common reference for evaluating the performance of equipment when subjected to high-energy disturbances on the power and interconnect lines. Figure 30 shows a circuit that was used to generate the combinational wave (hybrid) pulse described in IEC1000-4-5. It is based on the circuit shown in Figure 1 of IEC1000-4-5 (1995-02). Such a generator produces a 1.2 μs/50 μs open-circuit voltage waveform and an 8 μs/20 μs short circuit current waveform, which is why it is referred to as a hybrid generator. The surge generator has an effective output impedance of 2 Ω. This is defined as the ratio of peak open-circuit voltage to peak short-circuit current.

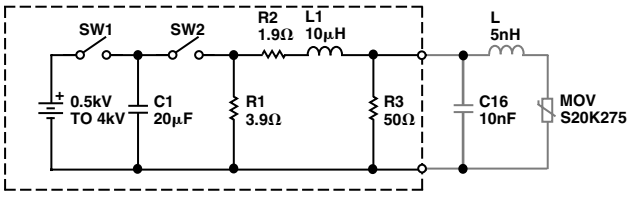


Figure 30. Surge Generator (IEC1000-4-5)

Figure 31 shows the generator voltage and current output waveforms. The characteristics of the combination wave generator are:

Open Circuit Voltage:
– 0.5 kV to at least 4.0 kV
– Waveform as shown in Figure 31
– Tolerance on open-circuit voltage is ±10%.

Short-Circuit Current:
– 0.25 kA to 2.0 kA
– Waveform as shown in Figure 31
– Tolerance on short-circuit current is ±10%.

Repetition rate of a least 60 seconds.

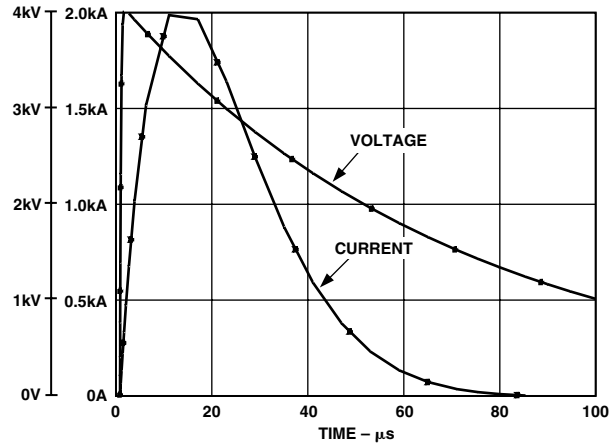


Figure 31. Open-Circuit Voltage/Short-Circuit Current

The MOV is very effective in suppressing these kinds of high energy/long duration surges. Figure 32 shows the voltage across the MOV when it is connected to the generator as shown in Figure 30. Also shown are the current and instantaneous power waveform. The energy absorbed by the MOV is readily estimated using the rectangle method as shown.

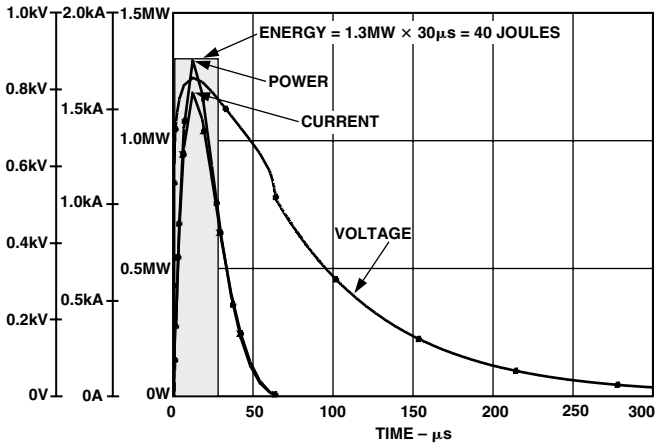


Figure 32. Energy Absorbed by MOV During 4 kV Surge

Derating the MOV Surge Current

The maximum surge current (and, therefore, energy absorbed) that an MOV can handle is dependant on the number of times the MOV will be exposed to surges over its lifetime. The life of an MOV is shortened every time it is exposed to a surge event. The data sheet for an MOV device will list the maximum nonrepetitive surge current for an 8 μs/20 μs current pulse. If the current pulse is of longer duration, and if it occurs more than once during the life of the device, this maximum current must be derated. Figure 33 shows the derating curve for the S20K275. Assuming exposures of 30 μs duration, and a peak current as shown in Figure 32, the maximum number of surges the MOV can handle before it goes out of specification is about 10. After repeated loading (10 times in the case just described) the MOV voltage will change. After initially increasing, it will rapidly decay.

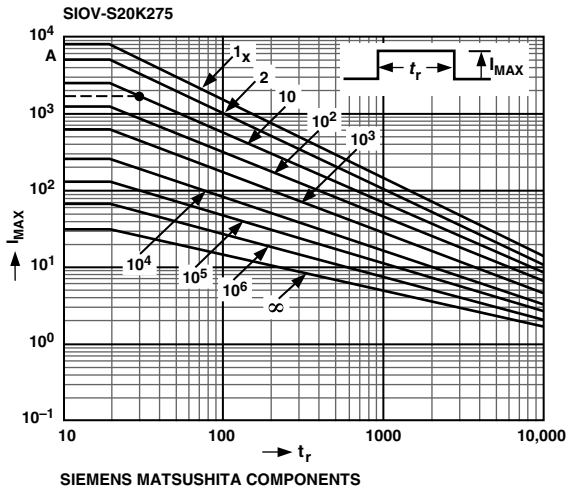


Figure 33. Derating Curve for S20K275

EMC Test Results

The reference design has been fully tested for EMC at an independent test house. Testing was carried out by Integrity Design & Test Services Inc., Littleton, MA 01460, USA. The reference design was also evaluated for Emissions (EN 55022 Class B) pursuant to IEC 1036:1996 requirements. A copy of the test report can be obtained from the Analog Devices website at:

http://www.analog.com/techsupt/application_notes/ad7755/64567_e1.pdf

The design was also evaluated for susceptibility to electrostatic discharge (ESD), radio frequency interference (RFI), keyed radio frequency interference, and electrical fast transients (EFT), pursuant to IEC 1036:1996 requirements. The test report is available at:

http://www.analog.com/techsupt/application_notes/ad7755/64567_c1.pdf

A copy of the certification issued for the design is shown in the test results section of this application note.

PCB DESIGN

Both susceptibility to conducted or radiated electromagnetic disturbances and analog performance were considered at the PCB design stage. Fortunately, many of the design techniques used to enhance analog and mixed-signal performance also lend themselves well to improving the EMI robustness of the design. The key idea is to isolate that part of the circuit that is sensitive to noise and electromagnetic disturbances. Since the AD7755 carries out all the data conversion and signal processing, the robustness of the meter will be determined to a large extent by how protected the AD7755 is.

In order to ensure accuracy over a wide dynamic range, the data acquisition portion of the PCB should be kept as quiet as possible, i.e., minimal electrical noise. Noise will cause inaccuracies in the analog-to-digital conversion process that takes place in the AD7755. One common source of noise in any mixed-signal system is the ground return for the power supply. Here high-frequency noise (from fast edge rise times) can be coupled into the analog portion of the PCB by the common impedance of the ground return path. Figure 34 illustrates the mechanism.

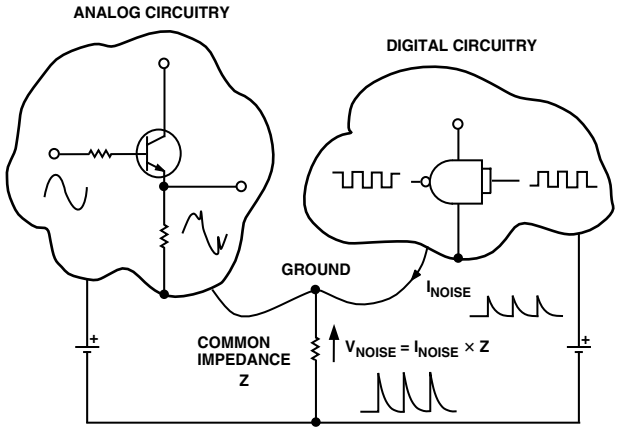


Figure 34. Noise Coupling via Ground Return Impedance

One common technique to overcome these kinds of problems is to use separate analog and digital return paths for the supply. Also, every effort should be made to keep the impedance of these return paths as low as possible. In the PCB design for the AD7755, separate ground planes were used to isolate the noisy ground returns. The use of ground plane also ensures the impedance of the ground return path is kept as very low.

The AD7755 and sensitive signal paths are located in a "quiet" part of the board that is isolated from the noisy elements of the design like the power supply, flashing LED, etc. Since the PSU is capacitor-based, a substantial current (approximately 32 mA at 220 V) will flow in the ground return back to the phase wire (system ground). This is shown in Figure 35. By locating the PSU in the digital portion of the PCB, this return current is kept away from the AD7755 and analog input signals. This current is at the same frequency as the signals being measured and could cause accuracy issues (e.g., crosstalk between the PSU as analog inputs) if care is not taken with the routing of the return current. Also, part of the attenuation network for the Channel 2 (voltage channel) is in the digital portion of the PCB. This helps to eliminate possible crosstalk to Channel 1 by ensuring analog signal amplitudes are kept as low as possible in the analog ("quiet") portion of the PCB. Remember that with a shunt size of 350 μΩ, the voltage signal range on Channel 1 is 35 μV to 14 mV (2% Ib to 800% Ib). Figure 35 shows the PCB floor plan which was eventually adopted for the watt-hour meter.

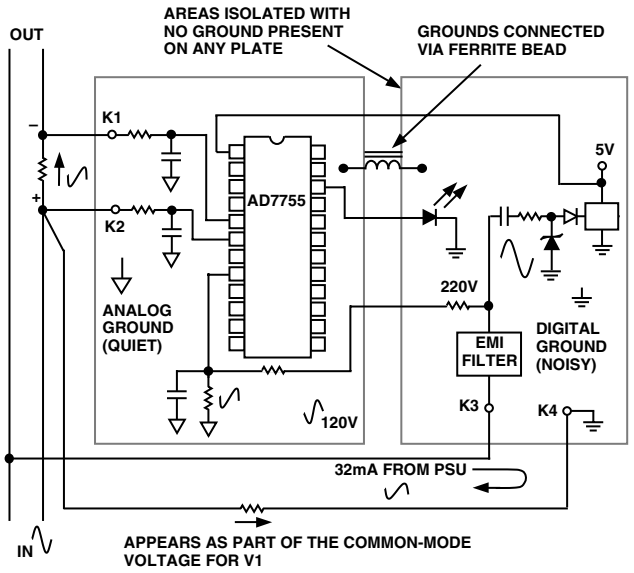


Figure 35. AD7755 Watt-Hour Meter PCB Design

The partitioning of the power planes in the PCB design as shown in Figure 35 also allows us to implement the idea of a "moat" for the purposes of immunity to electromagnetic disturbances. The digital portion of the PCB is the only place where both phase and neutral wires are connected. This portion of the PCB contains the transience suppression circuitry (MOV, ferrite, etc.) and power supply circuitry. The ground planes are connected via a ferrite bead that helps to isolate the analog ground from high-frequency disturbances (see Design For Immunity to Electromagnetic Disturbances section).

METER ACCURACY/TEST RESULTS

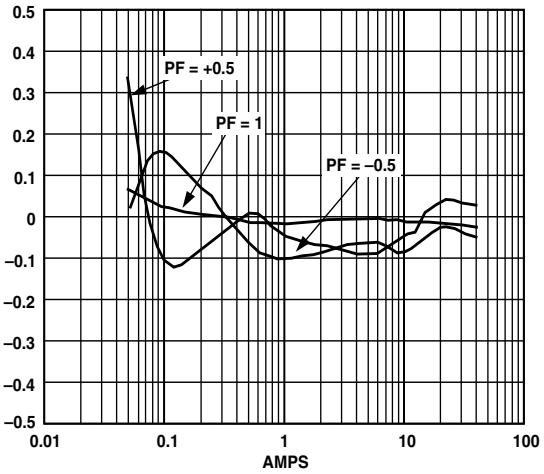


Figure 36. Measurement Error (% Reading) @ 25°C, 220 V, PF = +0.5/–0.5, Frequency = 50 Hz

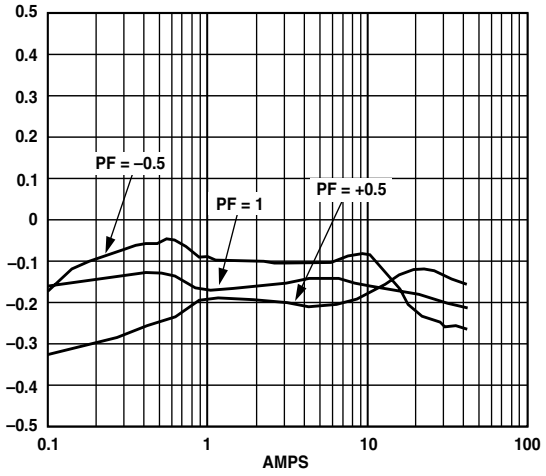


Figure 37. Measurement Error (% Reading) @ 70°C, 220 V, PF = +0.5/–0.5, Frequency = 50 Hz

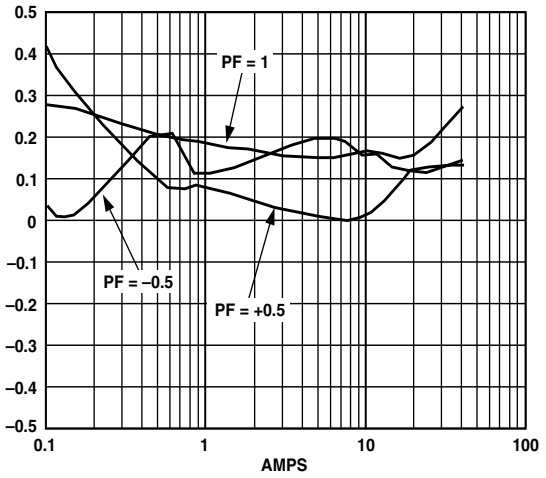


Figure 38. Measurement Error (% Reading) @ –25°C, 220 V, PF = +0.5/–0.5, Frequency = 50 Hz

EMISSIONS TESTING (EMC) N55022:1994
At end of data sheet.

SUSCEPTIBILITY TESTING (EMC) EN 61000-4-2, EN 61000-4-3, EN 61000-4-4, ENV 50204
At end of data sheet.

ANSI C12.16 AND IEC1039
The ANSI standard governing Solid-State Electricity Meters is ANSI C12.16-1991. Since this application note refers to the IEC 1036 specifications when explaining the design, this section will explain some of those key IEC1036 specifications in terms of their ANSI equivalents. This should help eliminate any confusion caused by the different application of some terminology contained in both standards.

Class—IEC1036

The class designation of an electricity meter under IEC1036 refers to its accuracy. For example a Class 1 meter will have a deviation from reference performance of no more that 1%. A Class 0.5 meter will have a maximum deviation of 0.5% and so on. Under ANSI C12.16 Class refers to the maximum current the meter can handle for rated accuracy. The given classes are: 10, 20, 100, 200 and 320. These correspond to a maximum meter current of 10 A, 20 A, 100 A, 200 A and 320 A respectively.

Ibasic (Ib)—IEC1036

The basic current (Ib) is a value of current with which the operating range of the meter is defined. IEC1036 defines the accuracy class of a meter over a specific dynamic range, e.g., 0.05 Ib $\leq$ I $\leq$ I_{MAX}. It is also used as the test load when specifying the maximum permissible effect of influencing factors, e.g., voltage variation and frequency variation. The closest equivalent in ANSI C12.16 is the Test Current. The Test Current for each meter class (maximum current) is given below:

Class 10 : 2.5 A
Class 20 : 2.5 A
Class 100 : 15 A
Class 200 : 30 A
Class 320 : 50 A

I_{MAX}—IEC1036

I_{MAX} is the maximum current for which the meter meets rated accuracy. This would correspond to the meter class under ANSI C12.16. For example a meter with an I_{MAX} of 20 A under IEC 1026 would be designated Class 20 under ANSI C12.16.

NO LOAD THRESHOLD

The AD7755 has on-chip anticreep functionality. The AD7755 will not produce a pulse on CF, F1, or F2 if the output frequency falls below a certain level. This feature ensures that the energy meter will not register energy when no load is connected. IEC 1036 (1996-09) section 4.6.4 specifies the start-up current as being not more that 0.4% Ib at PF = 1. For this design the start current is calculated at 7.8 mA or 0.16% Ib—see No Load Threshold section in the AD7755 data sheet.

Bill of Materials

Part(s)	Details	Comments
R1, R2, R3, R4	1 kΩ, 1%, 1/8 W	SMD 1206 Resistor Surface Mount, Panasonic ERJ-8ENF1001 Digi-Key No. P 1K FCT-ND
R5	300 kΩ, 5%, 1/2 W, 200 V	SMD 2010 Resistor Surface Mount, Panasonic, ERJ-12ZY304 Digi-Key No. P 300K WCT-ND
R6	150 kΩ, 5%, 1/2 W, 200 V	SMD 1210 Resistor Surface Mount, Panasonic, ERJ-14YJ154 Digi-Key No. P 150K VCT-ND
R7	75 kΩ, 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ753 Digi-Key No. P 75K ECT-ND
R8	39 kΩ, 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ393 Digi-Key No. P 39K JCT-ND
R9	18 kΩ, 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ183 Digi-Key No. P 18K JCT-N
R10	9.1 kΩ, 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ912 Digi-Key No. P 9.1K JCT-ND
R11	5.1 kΩ, 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ512 Digi-Key No. P 5.1K JCT-ND
R12	2.2 kΩ, 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ222 Digi-Key No. P 2.2K JCT-ND
R13	1.2 kΩ, 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ122 Digi-Key No. P 1.2K JCT-ND
R14	560 Ω, 5%, 1/16 W, 50 V	SMD 0402 Resistor Surface Mount, Panasonic, ERJ-2GEJ561 Digi-Key No. P 560 JCT-ND
R15, R16	330 kΩ, 5%, 1/2 W, 200 V	SMD 2010 Resistor Surface Mount, Panasonic, ERJ-12ZY334 Digi-Key No. P 330K WCT-ND
R17, R23	1 kΩ, 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ102 Digi-Key No. P 1K ECT-ND
R18	820 Ω, 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ821 Digi-Key No. P 820 ECT-ND
R19, R20	20 Ω, 5%, 1/8 W, 200 V	Resistor Surface Mount, Panasonic, ERJ-8GEYJ200 Digi-Key No. P 20 ECT-ND
R21	470 Ω, 5%, 1 W	Through-hole, Panasonic, Digi-Key No. P470W-1BK-ND
R22	10 Ω, 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ100 Digi-Key No. P 10 ECT-ND
C1, C2, C3, C4	33 nF, Multilayer Ceramic, 10% 50 V, X7R	SMD 0805 Capacitor Surface Mount, Panasonic, ECJ-2VB1H333K Digi-Key No. PCC 1834 CT-ND
C5, C13	10 μF, 6.3 V	EIA size A Capacitor Surface Chip-Cap, Panasonic, ECS-TOJY106R Digi-Key No. PCS 1106CT-ND – 3.2 mm × 1.6 mm

Part(s)	Details	Comments
C6, C7, C10, C12, C14, C15, C19	100 nF, Multilayer Ceramic, 10%, 16 V, X7R	SMD 0805 Capacitor Surface Mount, Panasonic, ECJ-2VB1E104K Digi-Key No. PCC 1812 CT-ND
C8, C9	22 pF, Multilayer Ceramic, 5%, 50 V, NPO	SMD 0402 Capacitor Surface Mount, Panasonic, ECU-E1H220JCQ Digi-Key No. PCC 220CQCT-ND
C11	6.3 V, 220 μF, Electrolytic	Through-hole Panasonic, ECA-OJFQ221 Digi-Key P5604 – ND D = 6.3 mm, H = 11.2 mm, Pitch = 2.5 mm, Dia. = 0.5 mm
C16	10 nF, 250 V, Class X2	Metallized Polyester Film Through-Hole Panasonic, ECQ-U2A103MN Digi-Key No. P4601-ND
C17	470 nF, 250 V AC	Metallized Polyester Film Through-Hole Panasonic, ECQ-E6474KF Digi-Key No. EF6474-NP
C18	35 V, 470 μF, Electrolytic	Through-Hole Panasonic, ECA-1VHG471 Digi-Key P5554 – ND
U1	AD7755AN	Supplied by ADI – 24 Pin DIP, Use Pin Receptacles (P1–P24)
U2	LM78L05	National Semiconductor, LM78L05ACM, S0-8 Digi-Key LM78L05ACM-ND
U3	PS2501-1	Opto, NEC, Digi-key No PS2501-1NEC-ND
U4	AD780BRS	Supplied by ADI – 8 Pin SOIC
D1	Low Current LED	HP HLMP-D150 Newark 06F6429 (Farnell 323-123)
D2	Rectifying Diode	1 W, 400 V, DO-41, 1N4004, Digi-Key 1N4004DICT-ND
D3	Zener Diode	15 V, 1 W, DO–41, 1N4744A Digi-Key 1N4744ADICT-ND
Z1, Z2	Ferrite Bead Cores	Axial-Leaded (15 mm × 3.8 mm) 0.6 mm Lead Diameter Panasonic, EXCELSA391, Digi-Key P9818BK-ND
Z3, Z4	Ferrite SMD Bead	SMD 1806 Steward, LI 1806 E 151 R Digi-Key 240-1030-1-ND
Y1	3.579545 MHz XTAL	Quartz Crystal, HC-49(US), ECS No. ECS-35-17-4 Digi-Key No. X079-ND
MOV1	Metal Oxide Varistors	AC 275 V, 140 Joules FARNELL No. 580-284, Siemens, S20K275
J1–J10	0.1 Ω, 5%, 1/4 W, 200 V	SMD 1210 Resistor Surface Mount, Panasonic ERJ-14RSJ0R1, Digi-Key No. P0.1SCT-ND
J11–J15	0 Ω, 5%, 1/8 W, 200 V	SMD 1206 Resistor Surface Mount, Panasonic, ERJ-8GEYJ000 Digi-Key No. P0.0ECT-ND
P1–P24	Single Low Profile	Sockets for U1 0.022'' to 0.025" Pin Diameter ADI Stock 12-18-33. ADVANCE KSS100-85TG
K1–K8	Pin Receptacles	0.037'' to 0.043'' Pin Diameter, Hex Press Fit Mil-Max no. 0328-0-15-XX-34-XX-10-0 Digi-Key ED5017-ND
Counter	2 Phase Stepper, 100 imp	China National Electronics Import & Export Shaanxi Co. No.11 A, Jinhua northern Road, Xi'an China. Email: chenyf@public.xa.sn.cn Tel: 86-29 3218247,3221399 Fax: 86-29 3217977, 3215870

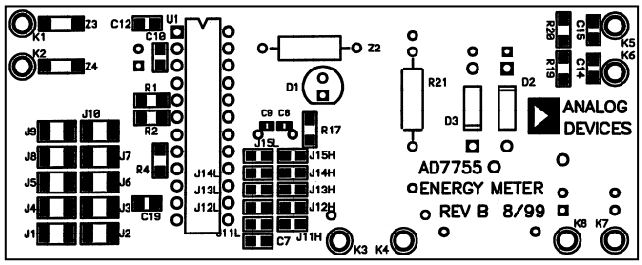


Figure 39. PCB Assembly (Top Layer)

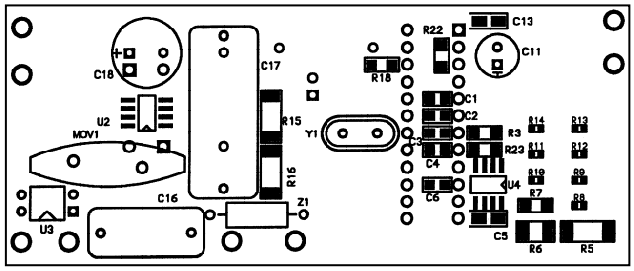


Figure 40. PCB Assembly (Bottom Layer)

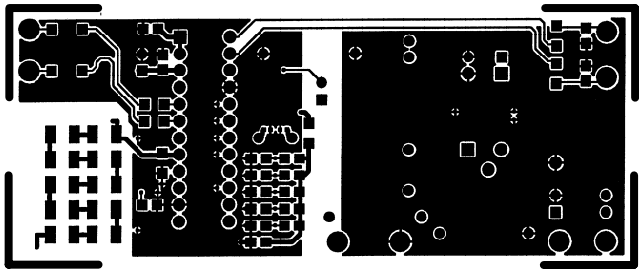


Figure 41. PCB (Top Layer)

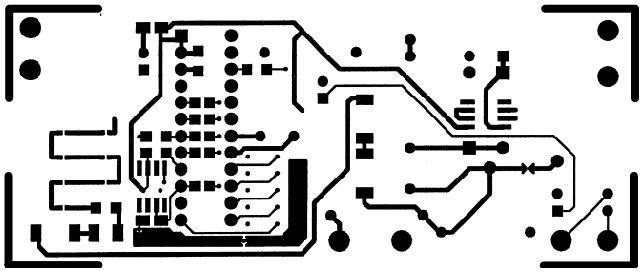


Figure 42. PCB (Bottom Layer)

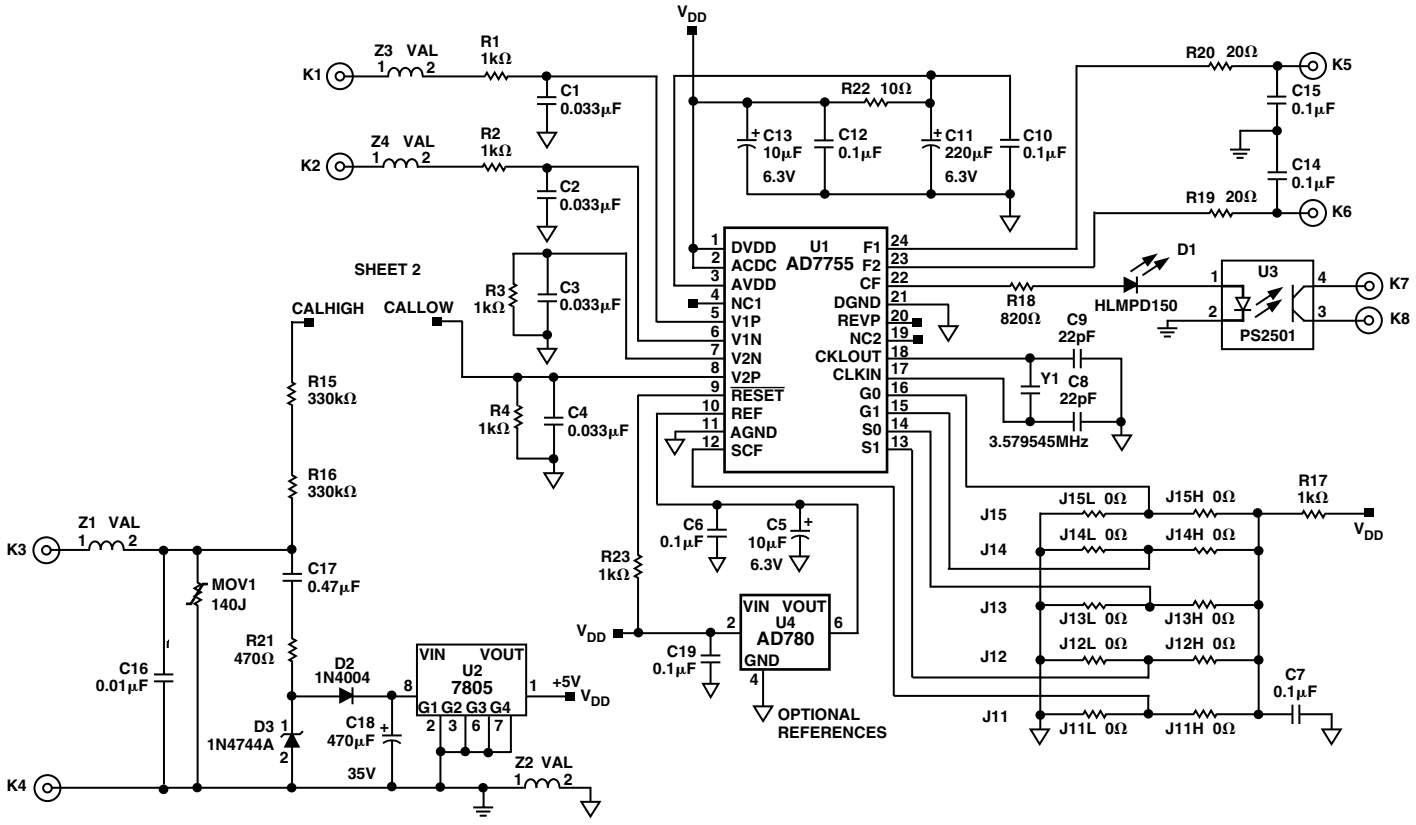


Figure 43. Schematic 1

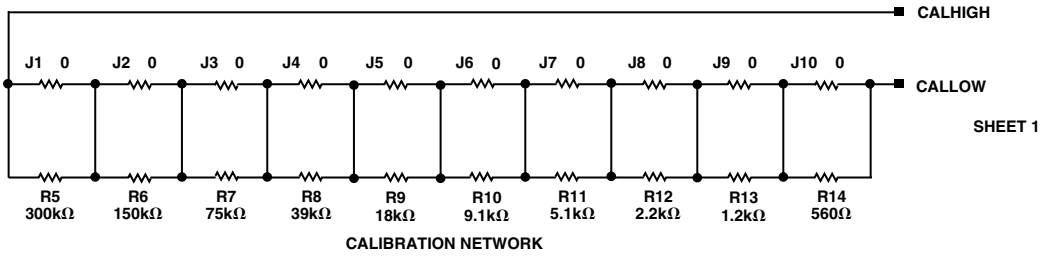


Figure 44. Schematic 2

Integrity
Design & Test
Services, Inc.

Certificate of Compliance

The following product was found to comply with the requirement stated below when tested in accordance with the test procedures described in the accompanying test/measurement report. Reference report number 64567.e1

Manufacturer:	Analog Devices, Inc. 804 Woburn Street Wilmington, MA 01887
Model:	Energy Meter (AD7755)
Requirement:	EN55022:1994 + A1:1995 + A2:1997, Class B
Applicable Directive:	89/336/EEC

Approved By:

Robert D. Goyette NVLAP Signatory	
Date	9/13/99

Remarks: *Testing is performed using calibrated equipment traceable to the National Institute of Standards and Technology (NIST).*

This certificate is valid for products tested as described in the accompanying test report. Specific modifications necessary to meet the above requirement, recommended by Integrity Design & Test Services, Inc. are described therein.

Integrity Design & Test Services, Inc. is accredited by the National Voluntary Laboratory Accreditation Program (NVLAP) for Electromagnetic Emissions Testing

Figure 45. Certificate 1, Emissions Testing

Integrity
Design & Test
Services, Inc.

Certificate of Compliance

The following product was found to comply with the requirement stated below when tested in accordance with the test procedures described in the accompanying test/measurement report. Reference report number 64567.c1

Manufacturer:	Analog Devices, Inc. 804 Woburn Street Wilmington, MA 01887
Model Number:	Solid State Energy Meter
Requirement:	EN 61000-4-2:1996, EN 61000-4-3:1996, ENV 50204:1993 and EN 61000-4-4:1995 (pursuant to IEC 1036:1996)
Applicable Directive:	89/336/EEC

Approved By:

Christopher P. Burch Immunity Section Manager	Christopher P. Burch
Date	9-13-99

Remarks: *Testing is performed using calibrated equipment traceable to the National Institute of Standards and Technology (NIST).*

This certificate is valid for products tested as described in the accompanying test report. Specific modifications necessary to meet the above requirement, recommended by Integrity Design & Test Services, Inc. are described therein.

E3742–2.5–6/00 (rev. A) 01017

PRINTED IN U.S.A.

Figure 46. Certificate 2, Susceptibility